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This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

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Massachusetts Institute of Technology
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Solid State Research

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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 2001. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

An aluminum-free $\lambda = 4$ μm laser has been demonstrated with 1.4 W/facet power and 13%/facet slope efficiency for a 2-mm cavity length under 1.8-μm diode pumping at $T = 78$ K. The fast-axis divergence is only ~10° full width at half-maximum.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

The residual phase noise of both fiber and semiconductor mode-locked lasers has been observed to be nearly independent of mode-locking frequency. The integrated phase noise (10 Hz to 10 MHz) of the fiber laser is 20–30× smaller than that of the semiconductor laser.

3. SUBMICROMETER TECHNOLOGY

A frequency selective surface (FSS) structure has been fabricated with optical lithography for use in a thermophotovoltaic system. The FSS provides a means for reflecting the unusable light below the bandgap of the thermophotovoltaic cell while transmitting the usable light above the bandgap.

An interference lithography system, operating at a 157-nm wavelength, has been constructed to demonstrate the resolution enhancement attainable using liquid immersion techniques. Dense arrays of 30-nm features have been patterned using this optical technique.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

Critical steps have been demonstrated in genetically engineering the bacteria used in novel biofuel cells that we are developeing. These fuel cells should have energy densities up to 60× greater than conventional batteries, and they could be refueled using almost any form of organic matter.

5. ADVANCED IMAGING TECHNOLOGY

To simplify fabrication of image sensors in a new merged charge-coupled device (CCD)/CMOS process, we have demonstrated a CCD fabricated in a single level of polysilicon. The results and simulations indicate good transfer efficiency with 0.3-μm gaps between the poly gates.

6. ANALOG DEVICE TECHNOLOGY

Experimental results obtained with Ni- and Zn-impurity-doped and oxygen deficient films have shown that disorder in the Cu-O planes or chains has a large influence on the nonlinear surface resistance. On the other hand, our results with Ca-doped films indicate that substitution on the Y sites seems to have little influence on the nonlinearities.

7. ADVANCED SILICON TECHNOLOGY

Sub-100-nm gates have been fabricated for fully depleted silicon-on-insulator CMOS transistor and circuit fabrication using optical lithography and a high-density, transformer-coupled plasma etch process. Transistors were fabricated with gate lengths of 25 and 50 nm.

REPORTS ON SOLID STATE RESEARCH

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PUBLICATIONS

Fabrication of Self-Aligned 90-nm Fully Depleted SOI CMOS SLOTFETs	C. K. Chen C-L. Chen P. M. Gouker P. W. Wyatt D. R. Yost J. A. Burns V. Suntharalingam M. Fritze C. L. Keast	*IEEE Electron Device Lett.* **22**, 345 (2001)
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Microcathodoluminescence of Impurity Doping at Gallium Nitride/Sapphire Interfaces	S. H. Goss* X. L. Sun* A. P. Young* L. J. Brillson* D. C. Look* R. J. Molnar	*Appl. Phys. Lett.* **78**, 3630 (2001)
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Periodically Poled $BaMgF_4$ for Ultraviolet Frequency Generation	S. C. Buchter T. Y. Fan V. Liberman J. J. Zayhowski	Conference on Lasers and Electro-Optics/ Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 6-11 May 2001
Ultrafast Lifetimes in Implanted Semiconductor Saturable Absorber Mirrors at 1.5 μm	J. P. Donnelly J. T. Gopinath* E. R. Thoen* E. M. Koontz* M. E. Grein* L. A. Kolodziejski* I. P. Ippen*	Conference on Lasers and Electro-Optics/ Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 6-11 May 2001

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† Titles of presentations are listed for information only. No copies are available for distribution.

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High-Performance Optically Pumped Band-IV Semiconductor Lasers Using an Integrated Absorber Structure Combined with Novel QW Active Regions	G. W. Turner M. J. Manfra A. K. Goyal P. J. Foti	Solid State Diode Laser Technology Review, Albuquerque, New Mexico, 21-24 May 2001
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Immersion Interference Lithography at 157 nm	M. Switkes M. Rothschild	45th International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication, Washington, D.C., 29 May–1 June 2001
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OMPVE Growth of Sb-Based III-V Materials for Thermophotovoltaics	C. A. Wang	3rd Workshop on the Fabrication, Characterization, and Applications of 6.1 Å III-V Semiconductors, Snowbird, Utah, 31 July–2 August 2001
High-Performance Optically Pumped Band-IV Semiconductor Lasers Using an Integrated Absorber Structure Combined with Novel QW Active Regions	G. W. Turner M. J. Manfra A. K. Goyal P. J. Foti	3rd Workshop on the Fabrication, Characterization, and Applications of 6.1 Å III-V Semiconductors, Snowbird, Utah, 31 July–2 August 2001

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1. QUANTUM ELECTRONICS

1.1 HIGH-PERFORMANCE ALUMINUM-FREE OPTICALLY PUMPED MID-INFRARED SEMICONDUCTOR LASERS

Mid-infrared lasers operating in the $\lambda \sim 3$–5 μm range are of interest for a variety of commercial and military applications. Optically pumped, GaSb-based semiconductor lasers with type-II InAs/InGaSb quantum well (QW) gain regions have recently demonstrated improved power, efficiency, beam quality, and temperature performance as compared to their double-heterostructure counterparts [1]–[3]. In particular, the integrated absorber laser design, which utilizes GaInAsSb absorber layers to absorb the pump radiation and then transfer electronic carriers to the QWs, has proven to have many advantages [3].

To our knowledge, all of the GaSb-based lasers grown to date, both electrically and optically pumped, have incorporated high aluminum mole fraction compounds in at least one of the layers. Since these compounds readily oxidize, fabrication of advanced device structures is complicated and care must be taken to protect the laser facets. Furthermore, when using high aluminum mole fraction compounds such as AlAsSb in the optical cladding layer to confine the mid-infrared optical mode, the refractive index step between the cladding and guiding layers is large. Because of this large index step, the optical mode is strongly confined to the waveguiding layer and the far-field divergence is very wide in the fast axis (in the plane perpendicular to the epitaxial layers). In fact, we have found that the fast-axis divergence in AlAsSb-clad laser structures can approach the theoretical maximum of 90° full width at half-maximum (FWHM).

We demonstrate that it is possible to create a mid-infrared laser structure which is free of aluminum by using GaSb as the optical cladding material in an integrated absorber laser structure. Based on previously published data at shorter wavelengths [4], the refractive index of the GaInAsSb used in these structures is extrapolated to be higher than that of GaSb by only $\Delta n \sim 0.06$ at $\lambda \sim 4$ μm. This index step is an order of magnitude smaller than when using the more conventional AlAsSb as the optical cladding. Since the far-field divergence varies as $\sim(\Delta n)^{1/2}$ for a given waveguide V-number (normalized frequency), one would expect a reduction in the far-field divergence of roughly 3×. Reducing the far-field divergence angle has numerous advantages such as (1) improved efficiency of collection optics, (2) reduced optical aberrations from the collection optics, and (3) the ability to create low-reflectivity facet coatings. One final advantage of the weaker optical confinement is the larger optical mode size. This reduces the modal overlap with each of the QW gain regions and thereby reduces the tendency for filament formation [5].

The GaSb-clad laser structure shown in Figure 1-1 was grown by solid-source molecular beam epitaxy. Ten type-II QWs, each consisting of 21-Å InAs/24-Å GaInSb/21-Å InAs, were embedded within the 1-μm-thick $Ga_{0.85}In_{0.15}As_{0.08}Sb_{0.92}$ absorber layers. A 4-μm-thick GaSb cap layer served as the top optical cladding while the GaSb substrate served as the lower cladding. No aluminum was used in the growth of this laser structure. The fast-axis far-field divergence is calculated to be ~22° FWHM assuming a refractive index difference between GaSb and GaInAsSb of $\Delta n = 0.06$.

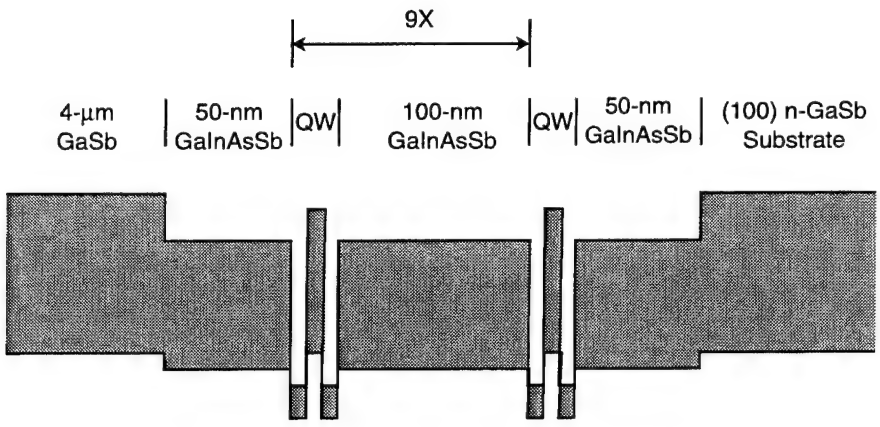

Figure 1-1. Schematic energy band diagram of GaSb-clad laser structure.

Uncoated, 2-mm-long lasers were mounted epi-side-up on a copper submount using thermal paste and then cooled in a liquid nitrogen dewar. Devices were optically pumped using an InGaAs/InP diode laser array operating at $\lambda = 1.8$ μm. Figure 1-2 plots the pulsed (35 μs, 2.5% duty cycle) single-facet output power vs input pump power at a heatsink temperature of 78 K. The $\lambda = 3.9$ μm, single-facet power was measured to be 1.4 W_{peak} at a pump power of 18 W_{peak}, and the initial slope efficiency is 13%/facet. As shown in Figure 1-3, the fast-axis far-field divergence is measured to be ~10° FWHM. This is narrower than the expected value. Also, the far-field profile is asymmetric for reasons that are under investigation. In any case, to our knowledge, this fast-axis far-field divergence is at least 4× smaller than any other value reported for a GaSb-based mid-infrared semiconductor laser [3]. The far-field divergence in the slow axis (in the plane parallel to the epitaxial layers) is measured to be less than 10° FWHM. We believe that the low confinement factor of this structure contributes to this reduced slow-axis divergence [6].

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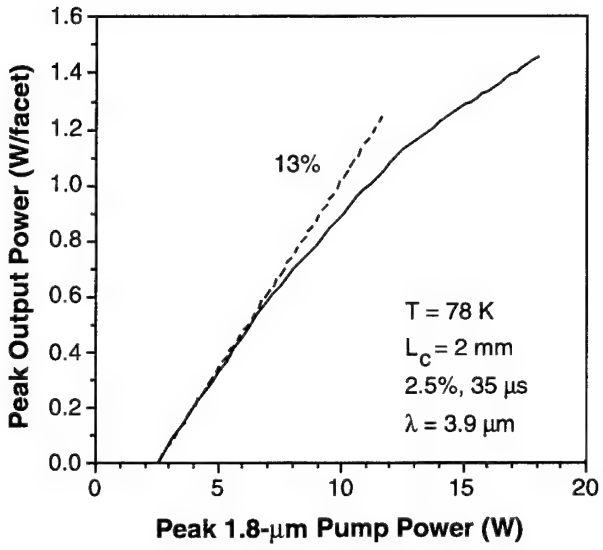

Figure 1-2. Output power vs pump power.

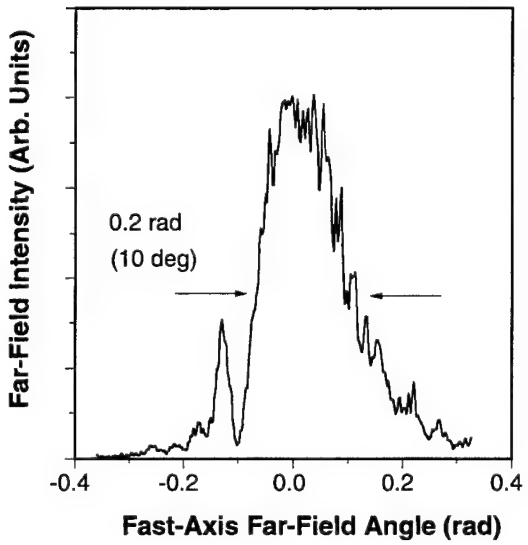

Figure 1-3. Fast-axis far-field divergence.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 RESIDUAL PHASE-NOISE MEASUREMENTS OF ACTIVELY MODE-LOCKED FIBER AND SEMICONDUCTOR LASERS

Actively mode-locked lasers are used in numerous applications, such as high-speed optical communications, laser radars, and photonic analog-to-digital conversion. In these applications, the timing jitter of the pulse train produced by the mode-locked laser can degrade system performance. This timing jitter can be quantified by measuring the phase noise of the detected laser pulse train.

The phase noise of both fiber and semiconductor mode-locked lasers has been measured using several techniques [1]–[3]. Most of the previously reported phase-noise measurements were accomplished using lasers mode locked at frequencies greater than 5 GHz. Here, we report residual phase-noise measurements of both actively mode-locked fiber and semiconductor lasers using sinusoidal mode-locking frequencies between 500 MHz and 5 GHz.

The fiber laser is a 1.55-μm polarization-maintaining erbium-doped fiber ring laser that is harmonically mode locked using a sinusoidal drive signal. The fundamental cavity frequency is 9.9 MHz. The temporal width of the output pulses ranged from 51 to 27 ps full width at half-maximum (FWHM) for mode-locking frequencies from 500 MHz to 5 GHz, respectively.

The mode-locked semiconductor laser uses an external cavity configuration. The laser's gain and modulator sections are monolithically integrated in a curved-channel ridge-waveguide geometry [4]. The active material is a step-graded-index separate-confinement heterostructure with five 8-nm InGaAsP quantum wells under 1% compressive strain, which were grown by organometallic vapor phase epitaxy [5]. The external cavity is defined by the front facet (output) of the semiconductor chip (30% reflectivity) and a grating mounted in the Littrow configuration. The reflectivity of the chip's rear facet was minimized by the combination of the curved waveguide and an antireflection coating. The cavity was configured for a fundamental mode-locking frequency of 500 MHz and a center wavelength of 1545 nm. The temporal pulse width of the output pulses was ~20 ps FWHM independent of mode-locking frequency.

As seen in Figure 2-1, the lasers were harmonically mode locked using an HP8665B synthesizer at frequencies between 500 MHz and 5 GHz. A 10-dB coupler connects the output of the synthesizer to the mode-locking input of the laser, as well as to the input of a variable delay. The output of the laser is detected, filtered, and amplified prior to the input of the HP3048A phase-noise measurement system. This system is used to compare the outputs of the laser and the frequency synthesizer using a phase detector driven in phase quadrature.

Figures 2-2(a) and 2-2(b) contain residual phase-noise measurement results for the fiber laser and the semiconductor laser, respectively. For each laser, these measurements were carried out at three different

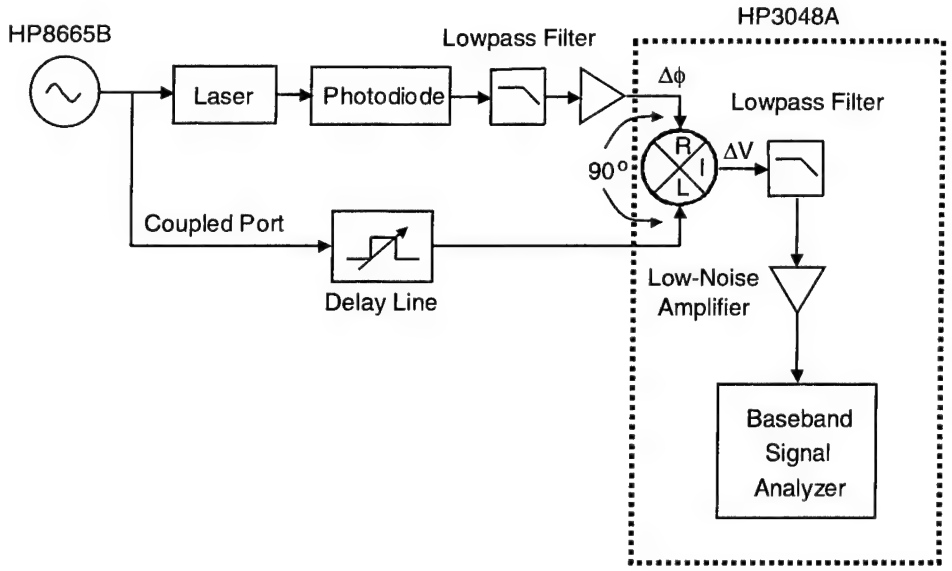

Figure 2-1. Block diagram of system used for residual phase-noise measurements.

mode-locking frequencies. For each phase-noise measurement, a corresponding timing jitter σ_T was calculated from the integrated phase noise using Equation (2.1). The fiber laser's supermode noise contribution was neglected.

$$\sigma_T = \left(\frac{1}{2\pi f_o}\right)\sigma_\phi = \left(\frac{1}{2\pi f_o}\right)\sqrt{2\int_{f_{\min}}^{f_{\max}} L(f)df} \tag{2.1}$$

where f_o is the mode-locking frequency, $f_{\min}$ is the lowest offset from the carrier, $f_{\max}$ is the highest offset from the carrier, and $L(f)$ is the single-sideband phase noise.

The data in Figure 2-2 show that $L(f)$ is approximately constant, independent of the mode-locking frequency. This result is summarized in Figure 2-3, where the lines represent the jitter as a function of frequency for a constant integrated phase-noise variance σ_ϕ, and the symbols represent calculations of jitter (integrated from 10 Hz to 10 MHz) for lasers at various mode-locking frequencies. Initial theoretical studies of a semiconductor laser model incorporating carrier dynamics have shown similar results [6].

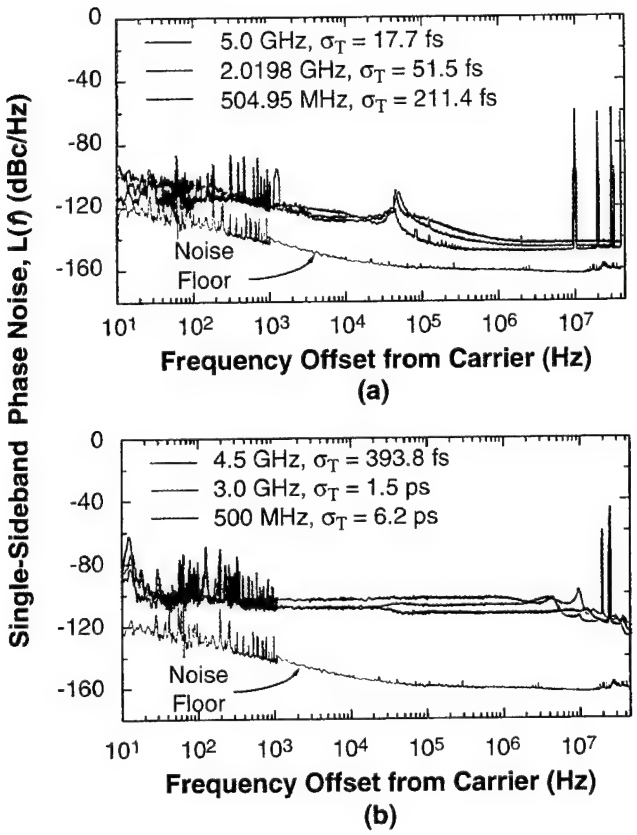

Figure 2-2. Laser residual phase-noise measurement results for various mode-locking frequencies. Laser jitter results are calculated from the integrated phase noise for frequency offsets between 10 Hz and 10 MHz: (a) fiber laser mode locking at frequencies of 504.95 MHz, 2.0198 GHz, and 5.0 GHz, (b) semiconductor laser mode locking at frequencies of 500 MHz, 3.0 GHz, and 4.5 GHz.

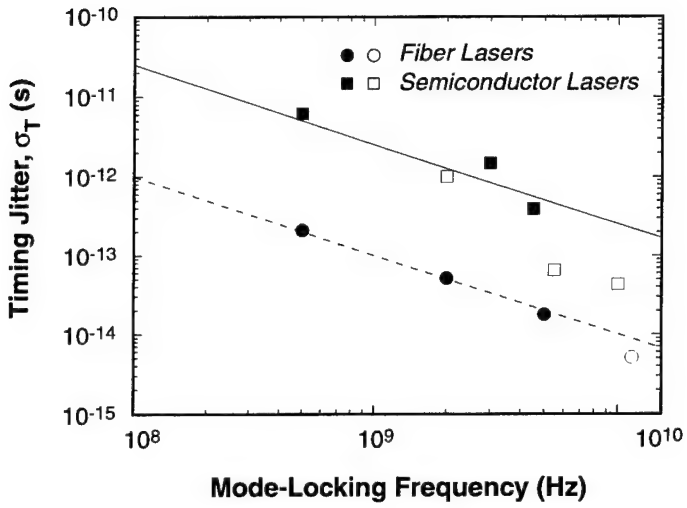

Figure 2-3 Timing jitter as function of frequency for different mode-locking frequencies. The lines in the graph represent the timing jitter as a function of frequency for a constant σ_ϕ. The closed symbols are the jitter results for the measured residual phase noise in Figure 2-2, and the open symbols are previously reported jitter results [1]–[3].

Residual phase-noise measurements and corresponding jitter calculations were made for both actively mode-locked fiber and semiconductor lasers. In the measurements reported here, the integrated phase noise of the fiber laser is a factor of 20–30× smaller than that of the semiconductor laser over narrowband integration limits (10 Hz to 10 MHz). Additionally, we have shown that the phase-noise spectrum for a given laser configuration is approximately independent of mode-locking frequency. This result indicates that the laser timing jitter scales inversely with mode-locking frequency. However, it is not known at this time if this scaling applies to larger offset frequencies. Experimental results have shown good agreement with initial theoretical results.

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3. SUBMICROMETER TECHNOLOGY

3.1 INFRARED FREQUENCY SELECTIVE SURFACES FABRICATED USING OPTICAL LITHOGRAPHY AND PHASE-SHIFT MASKS

Frequency selective surfaces (FSSs) provide a method for constructing a mirror whose reflection and transmission properties vary with wavelength but are relatively insensitive to the angle of incidence. The FSS demonstrated here is a type of wavelength selective filter which can be used to increase the efficiency of a thermophotovoltaic (TPV) system. In such a system, electricity is produced by converting infrared radiation from a heat source into electricity using a compound semiconductor TPV cell. Such a cell can only convert light with a wavelength shorter than the bandgap λ_g of the cell. To improve the efficiency of the system, a FSS is placed between the heat source and the TPV cell. The FSS reflects light with a wavelength longer than λ_g into the heat source rather than wasting this energy.

The design for the FSS contains a hexagonal array of circular slits or rings spaced by 1100 nm, center to center. The diameter and the linewidths of the circular slits are nominally 900 and 100 nm, respectively. Another common geometry used in FSSs is the cross-dipole structure [1],[2]. However, the ring structure is believed to be a better choice for TPV applications because the ring geometry is less sensitive to polarization and the angle of incidence [3]. The resonant wavelength of a freestanding ring structure can be estimated as being equal to the ring's circumference [4]. When placed on a substrate, the resonant wavelength is shifted by an effective refractive index which is a combination of the indices of the substrate and the air above the FSS, giving the expression

$$\lambda_{\text{res}} = C\left[\left(n_1^2 + n_2^2\right)/2\right]^{1/2} \tag{3.1}$$

where λ_{res} is the resonant wavelength, n_1 and n_2 are the refractive indices of the air above the FSS and of the substrate, and C is the circumference of the ring structures. By using Equation (3.1), the estimated resonant wavelength of the ring structures described above is 7 μm. Because the FSS design contains circular slits cut into an otherwise reflective metal film, the resonant behavior of the FSS allows transmission of light that is near the resonant wavelength. Away from the resonance, the FSS reflects the light.

The fabrication of the FSS was done using deep-uv lithography and a chromeless phase-shift mask. The use of phase-shift masks in optical lithography is a resolution enhancement technique which has demonstrated feature sizes as small as 50 nm [5]. In this technique a chromeless mask with an etched 180° phase step is used. When projected, the phases from each side of the step destructively interfere producing a narrow dark line. The width of this line is given by the formula:

$$w_{\text{FWHM}} = \frac{0.25\lambda}{\text{NA}} \tag{3.2}$$

where w_{FWHM} is the width of the dark line (full width at half-maximum) and NA is the numerical aperture of the projection system. Although phase-shift masks have the ability to create narrow lines, this simple chromeless mask technique is constrained to only create lines that follow nonintersecting closed paths. The ring structures fabricated here do not violate this constraint and are ideally suited for fabrication with phase-shift masks.

The process for fabricating the FSSs consisted of a single lithography step followed by metallization and liftoff. First, UV5 photoresist (manufactured by Shipley) 465 nm thick was applied to silicon wafers. Standard process conditions for the photoresist were used, with one notable exception. Before post-exposure bake the sample was dipped in a weak base solution consisting of one part 0.26-M TMAH in 100 parts deionized water. This weak base creates a thin inhibition layer at the top surface of the photoresist. This inhibition layer develops to a slightly smaller feature size, creating a reentrant or T-topped profile. The profile improves liftoff by preventing the coating of the sidewalls of the resist during metallization. Metallization was done by electron beam evaporating 80 or 100 nm of gold or aluminum. A 5-nm evaporation of Ti preceded the gold evaporation to improve adhesion. Liftoff was done using warm ACT1 stripper with ultrasonic agitation.

The reticle was designed with both circular and hexagonal features with various widths. Figure 3-1 shows a series of scanning electron micrographs (SEMs) of resist summarizing results from these tests. Hexagons with widths of 880 and 900 nm could not produce rings that could be resolved. The 870-nm-wide hexagons and 870-nm-diam circles both successfully printed resolved rings, but the circles produced rings of much higher quality. The 900-nm circles nearly produced resolved rings. At a dose sufficient to produce the gap between the rings, the rings would start to have breaks in them. In all but the 870-nm circle images, there is a hexagonal structure visible. This hexagonal structure does not correspond to the hexagons of the mask, but is actually rotated 30° from the angle of the hexagons in the masks. The cause of this hexagonal artifact is the limited spatial resolution of the exposure system.

For further inspection, a sample with the pattern in resist was cross sectioned and imaged. An SEM of the cross-sectioned resist is shown in Figure 3-2. This image along with all the following results were obtained from the 870-nm (diameter) circle region of the mask. Because no antireflection coating was used, the reflection from the silicon substrate caused strong standing waves that resulted in the bands in the photoresist. Also visible in the figure is the desired T-topping. Although the T-topping is subtle, with only about 10 nm of overhang, this is sufficient to provide good liftoff. (A much larger overhang is undesirable and would result in a loss of resolution of the process). The cylindrical structures in Figure 3-2 appear to be cone shaped; the rings appear narrower at the top than at the bottom. This shape is believed to be an artifact of the SEM imaging process. If this were the true shape of the resist, it is unlikely that the liftoff procedure would have been so successful.

Figure 3-3 shows the final FSS after metallization and liftoff. In this picture the FSS is constructed of an 80-nm-thick gold layer. Similar results were obtained with aluminum and gold films 100 nm thick. The measured performance of a gold FSS, 100 nm thick, is shown in Figure 3-4. In the figure the transmission at normal incidence is plotted along with the reflection at near normal incidence (11°). The FSS is

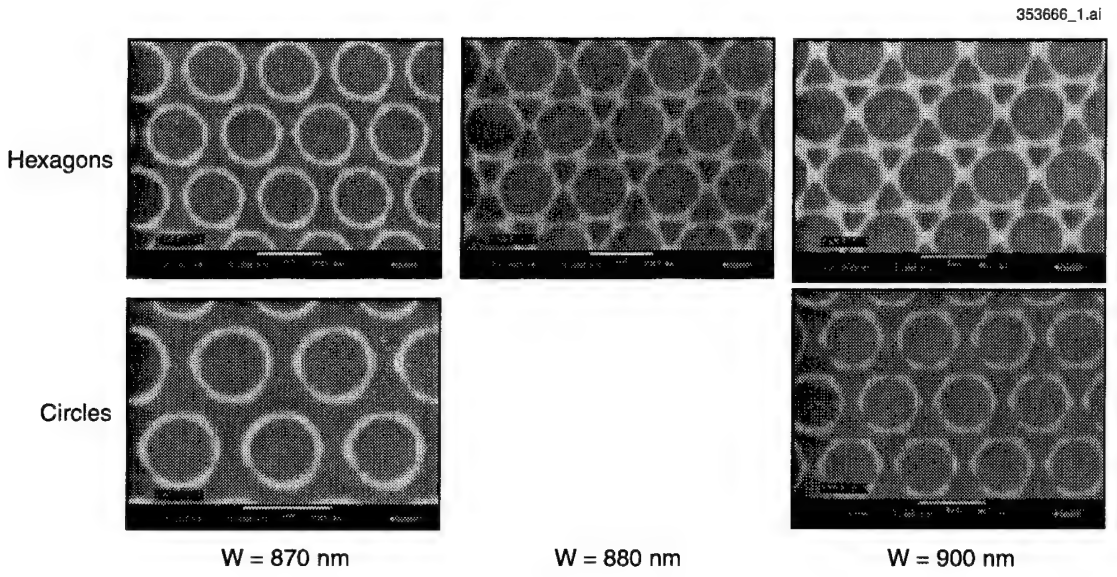

Figure 3-1. Experimental demonstration of printability of mask features. The top row contains examples of printing from the hexagon features on the mask with widths of 870, 880, and 900 nm. The bottom row contains examples of printing from the circular features on the mask with diameters of 870 and 900 nm.

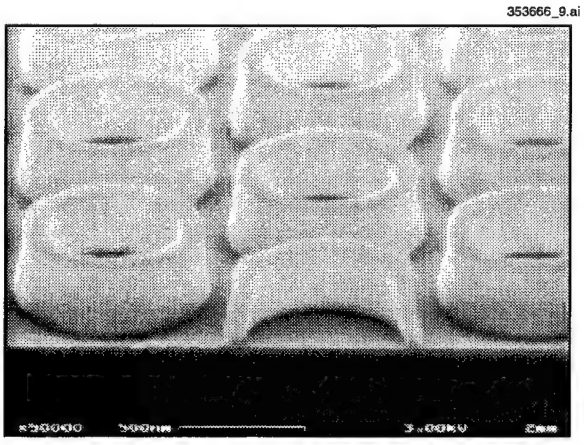

Figure 3-2. Scanning electron microscope (SEM) image of cross section of ring structures fabricated in resist. Visible are the desired small amount of T-topping and standing waves. The cone-like shape of the rings is believed to be an artifact caused by the SEM exposure of the resist.

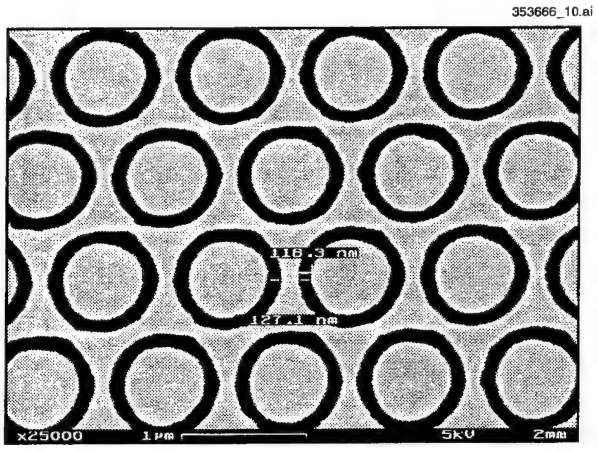

Figure 3-3. Top-down SEM image of frequency selective surface (FSS) fabricated in gold, 80 nm thick.

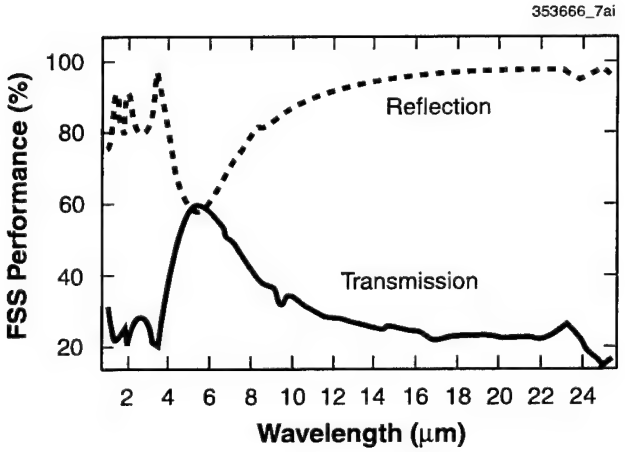

Figure 3-4. Performance of gold FSS at normal and near normal incidence. The FSS shows a band of transmission at 5 µm and reflection at other wavelengths.

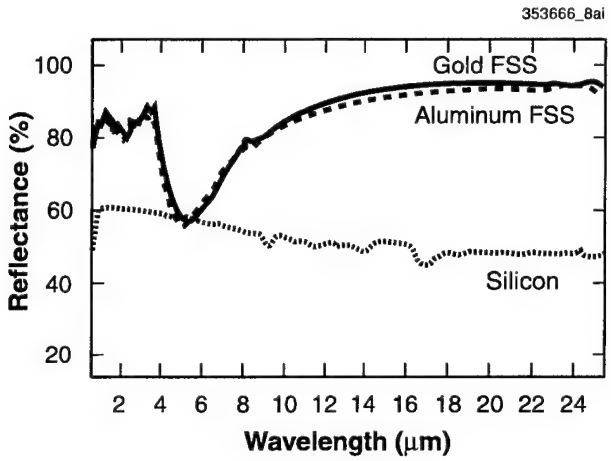

Figure 3-5. Reflectance of gold FSS, aluminum FSS, and silicon wafer at 45° incidence. Similar performance is shown for both materials. Also, the performance is similar to the performance demonstrated at near normal incidence in Figure 3-4.

reflective at longer wavelengths and becomes transmissive near a wavelength of 5 μm. At wavelengths much shorter than 5 μm the FSS is primarily reflective again. Thus the FSS performs as expected, except that the resonant wavelength is shifted slightly from the estimated wavelength of 7 μm.

The reflectance of FSSs constructed of gold and aluminum was measured and compared as shown in Figure 3-5. This time the reflectance was measured at an incident angle of 45°. There is little difference between the aluminum and gold FSSs, demonstrating that both materials are suitable for use at these wavelengths. Also, the measured reflectance at near normal incidence and at 45° both show a minimum at 5 μm demonstrating the desired insensitivity to angle. The reflectance of a similar bare silicon substrate is also plotted on the same graph. The silicon substrate is not ideal for this application because its reflectance is nearly 50% throughout the wavelength range of interest. It is likely that the use of silicon is limiting the reflectance dip (and transmission peak) to only reach ~50%.

The performance of the FSS can be enhanced by the use of multiple FSS layers [6],[7]. The use of aluminum as the metal for the FSS should allow the fabrication of multiple aluminum and SiO_2 layers using slightly modified standard microelectronic fabrication processes. Above it was demonstrated that aluminum performs nearly identically to gold at wavelengths >1 μm, making it a suitable choice for this application.

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3.2 IMMERSION LITHOGRAPHY AT 157 nm

Photolithography has been the mainstay of semiconductor device patterning for the last two decades and is expected to continue in a critical role at least to 70 nm and possibly beyond. Three trends developing in parallel have enabled this remarkable progress: (1) reduction in wavelength from mercury g-line (436 nm) to the 157-nm excimer laser, (2) increase in the NA of projection systems from ~0.35 to over 0.7, and (3) implementation of resolution enhancement techniques such as phase-shifting masks and off-axis illumination. Consideration has also been given to a more radical approach to improving resolution, immersion lithography [8]–[11] in which the space between the final optical element and the substrate is filled with a high index medium. In analogy with immersion microscopy, this has traditionally been understood to improve resolution by increasing NA. An equally valid and often more convenient way of understanding immersion lithography [12] is to consider an effective wavelength

$$\lambda_{\text{eff}} = \lambda_0 / n \tag{3.3}$$

where λ_0 is the vacuum wavelength and n is the index of the immersion medium. This gives a resolution

$$W = k_1 \frac{\lambda_{\text{eff}}}{\sin\theta_0} \tag{3.4}$$

where θ_0 is the angular half-aperture of the lens. This treatment emphasizes an advantage of immersion lithography over increases in "dry" NA; in immersion lithography, the decrease in depth of focus

$$\text{DOF} \propto \frac{W}{\text{NA}} \propto \frac{\lambda_{\text{eff}}}{\text{NA}^2} \tag{3.5}$$

is only linear with the increase in resolution rather than quadratic as with increase in NA.

Immersion lithography has previously been demonstrated [8] at wavelengths as low as $\lambda_0 = 257$ nm with $n = 1.5$ or $\lambda_{\text{eff}} = 171$ nm. However, to be of interest for semiconductor manufacturing, it must provide resolution beyond current or soon-to-be-available conventional techniques. A system with $\lambda_0 = 157$ nm and $n = 1.37$ such as we present here has an effective wavelength of 115 nm, a larger gain than the transition from 193 to 157 nm, and should enable projection imaging with dense features as small as 50 nm with NA = 0.9 and $k_1 = 0.4$. Because the vacuum wavelength remains unchanged, much of the work on sources, optical materials and designs, resists, contamination, etc. already done for 157-nm lithography translates directly to immersion lithography, greatly reducing the effort required to implement it.

The first step in implementing immersion lithography at 157 nm is the identification of a suitable immersion fluid. Such a fluid must be transparent enough to allow a working distance of at least 10s of μm, must be free of optical defects, and must not interact with the resist to impede image formation. In

addition, it must be compatible with the clean room environment and the semiconductor manufacturing process as well as nontoxic and chemically inert. Ideally, the liquid should also be index matched to CaF_2 optics (i.e., $n = 1.56$) and resistant to laser damage. We have identified a class of commercially available materials, perfluoropolyethers (PFPEs), which satisfy many of these requirements and are certainly adequate for these initial studies. PFPEs are widely available as oils and lubricants under the trade name Fomblin® (Ausimont Corp.). We have tested samples of two different PFPE materials, Fomblin Y and Fomblin Z. Unless otherwise noted, tests were carried out on the Y-18 and Z-25 grades as received.

The most important characteristic of an immersion fluid is its transparency. Measurements of the transmission of liquid layers of various thicknesses sandwiched between two CaF_2 windows yield the absorbance shown in Figure 3-6. Both grades of Fomblin have 157-nm absorbance $\alpha_{157} \cong 10^{-3}\ \mu m^{-1}$ base 10 which is ~1000× lower than current experimental 157-nm resists [13] and ~10× lower than 157-nm pellicle materials [14]. This allows a working distance on the order of 50 μm with ~90% transmission. The absorbance of Fomblin Y is slightly lower. In addition, the shoulder of the absorbance curve appears just above 157 nm leading to the expectation that chemical modification could move it below 157 nm, yielding a fluid with dramatically lower absorbance. The optical quality of these fluids is also good. Figure 3-7 shows the far-field scattering of light transmitted through a 50-μm layer of fluid between two CaF_2 windows. Fomblin Y contributes negligible scatter to that of the baseline empty cell while the additional scatter from Fomblin Z is roughly equivalent to 5 nm of surface roughness.

The resistance of the fluids to laser damage is illustrated in Figure 3-8. A 150-μm-thick layer of each fluid was irradiated at 157 nm. Fomblin Z is more damage resistant, with a 157-nm transmission drop of 17% for a dose of 100 J cm^{-2} at a fluence of 0.3 mJ cm^{-2} $pulse^{-1}$. For the same dose, the transmission of Fomblin Y, which is initially higher, drops over 80%. The damage to either fluid in the dose required to expose a single field, ~1 mJ cm^{-2}, is negligible. However, the damage resistance of the fluid will influence its handling. An easily damaged fluid would likely travel with the wafer, providing a fresh volume for each exposed field. On the other hand, a damage-resistant fluid could be part of the exposure tool, being replenished only as it is consumed.

The indices of refraction of Fomblin Y and Z are not as well matched to CaF_2 as might be hoped. The indices derived from spectroscopic ellipsometry are shown in Figure 3-9 with $n_{157} = 1.35$ and 1.37 for Fomblin Z-25 and Y-18, respectively, and 1.38 for Fomblin Y-140, a higher molecular weight version. Here again, we envision that suitable chemical modification could increase this index and thus improve the resolution of immersion lithography.

Finally, PFPEs have the advantage of being relatively chemically inert, nontoxic, and noncorrosive and thus compatible with the clean room environment and the semiconductor manufacturing process. Indeed, Fomblin is already present as pump oil in many clean rooms. We are currently studying the possible interactions of Fomblin with experimental 157-nm photoresists. For at least one resist, LUVR 99071, an ESCAP type resist [8] formulated for tool testing at 157 nm, it is clear that exposure to PFPEs neither swells nor dissolves the resist. Further studies are necessary to elucidate its impact, if any, on the imaging properties of the resist.

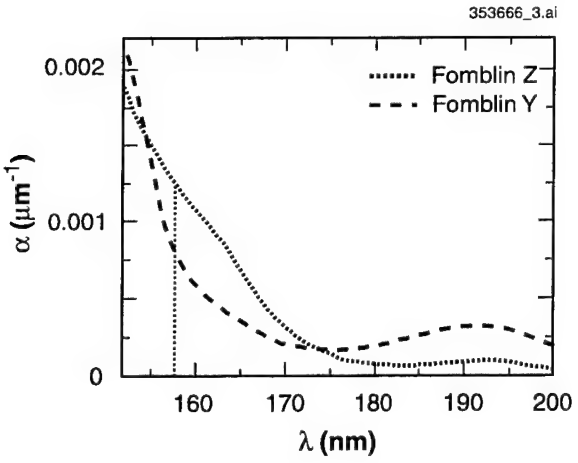

Figure 3-6. Absorbance of the unirradiated perfluoropolyether compounds Fomblin Y and Z as a function of wavelength.

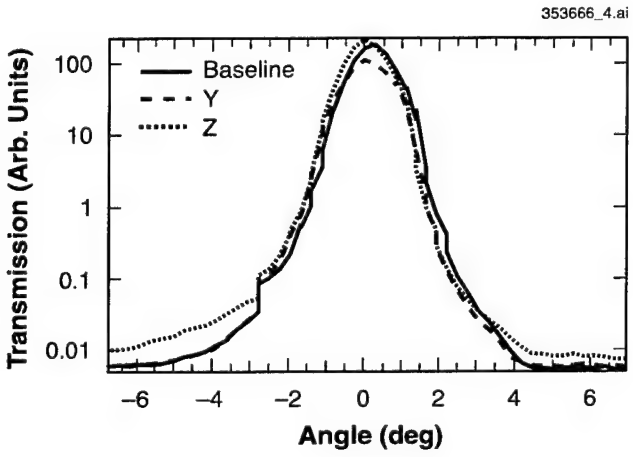

Figure 3-7. Far-field scattering of a cell consisting of 50 μm of immersion liquid (Fomblin Y or Z) sandwiched between two CaF_2 windows. The baseline is a cell with 50 μm of N_2 between the windows. Fomblin Y shows negligible scattering while Fomblin Z has scattering roughly equivalent to a 5-nm surface roughness. The sharp kink at –2.75° is an artifact of the measurement.

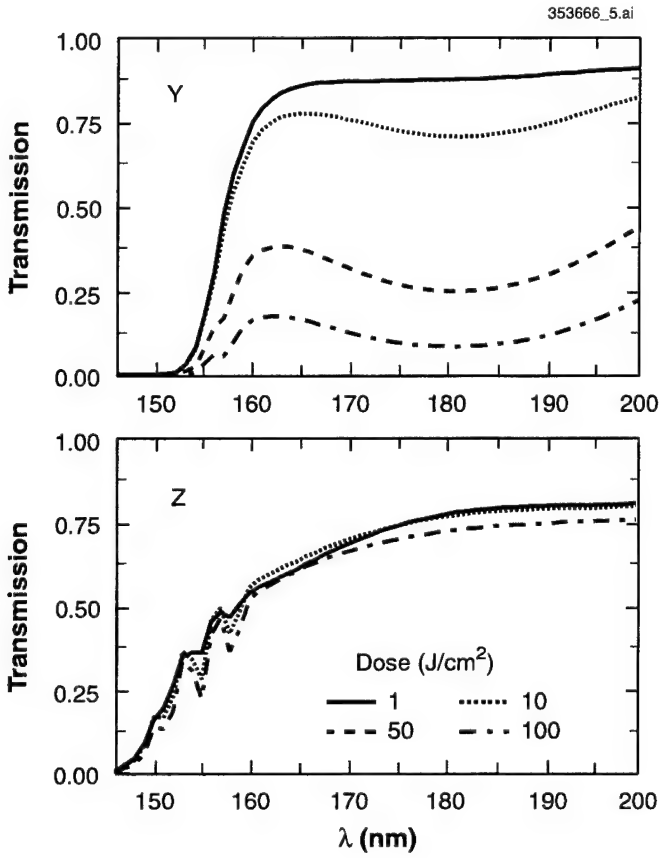

Figure 3-8. Spectrum of a 150-μm layer of Fomblin Y (top) and Z (bottom) between two CaF_2 windows after various doses of 157-nm irradiation.

The initial immersion lithography platform is a high-resolution lens-less interference lithography tool similar to the dry tool described in [15]. In interference lithography, two mutually coherent beams intersect at the surface of a resist-coated substrate forming a line and space pattern with a spatial period

$$\Lambda = \frac{\lambda_0}{2n\sin\theta} \tag{3.6}$$

where 2θ is the angle of intersection of the beams in air. In our design, $\theta = 60°$. This design was chosen for its ease of implementation with no mask, coatings, or curved optics, and its ease of adaptation to immersion lithography.

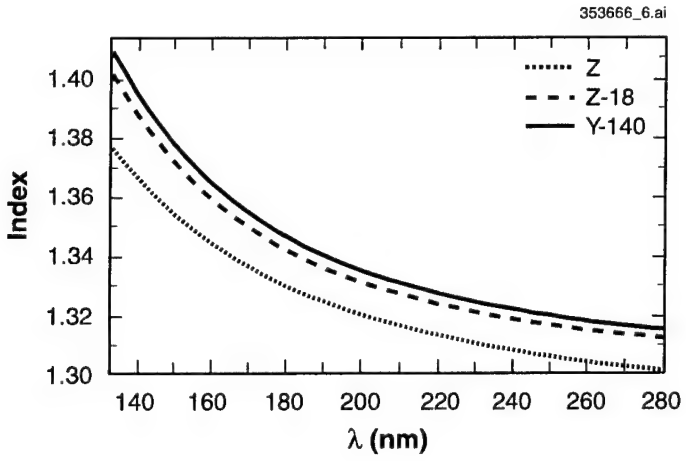

Figure 3-9. Index of refraction of two Fomblin compounds at three molecular weights determined by spectroscopic ellipsometry.

As pointed out in [8], it is the index of the final optic itself rather than that of the index matching fluid which decreases the spatial period of Equation (3.6). This can be understood by noting that a change in the index of the fluid will change both the effective wavelength and $\sin\theta$ by a factor of n, leaving Λ unchanged. The liquid thus serves only to allow the beams to exit the final optic at high θ without being totally internally reflected. The largest possible θ and thus the ultimate resolution is set by the critical angle at the optic-fluid interface (or the fluid-resist interface if $n_{\text{fluid}} > n_{\text{resist}}$), just as in projection imaging.

Thin layers (~55 nm) of LUVR 99071 resist [16] were spun on hexamethyldisilazane (HMDS)–treated Si substrates and baked at 130°C for 60 s. The substrate was then covered with a thin layer of immersion fluid and brought to within 50 μm of the CaF_2 trapezoid. After exposure, the sample was soaked for 3 min and then rinsed in Fomblin PFS-1, a low molecular weight PFPE solvent, to remove the immersion liquid. This was followed by the standard 90-s post-exposure bake at 130°C and 15-s soak in 0.26-N tetramethyl ammonium hydroxide (TMAH) developer. The SEM of an exposure is seen in Figure 3-10, showing a line and space pattern with Λ = 60 nm, as expected from Equation (3.6) with n = 1.56 for the CaF_2 prism.

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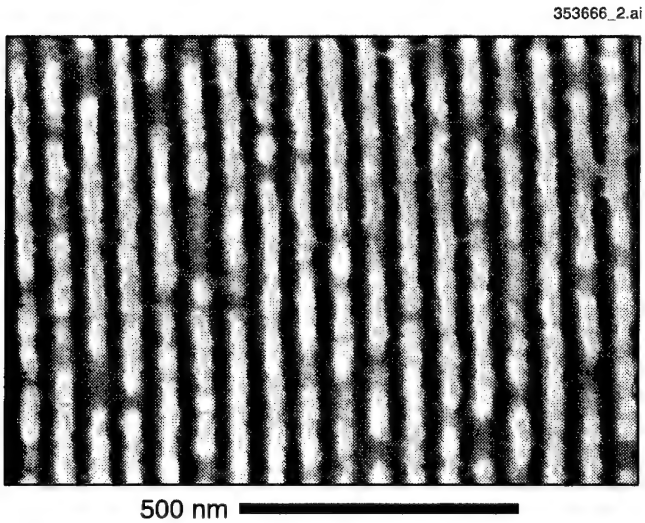

Figure 3-10. SEM of a thin layer of LUVR 99071 resist exposed in the immersion interference lithography system.

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 HIGH-ENERGY BIOFUEL CELL WITH ENGINEERED ELECTROCYTE LAYERS

The objective of this project is to develop biologically based fuel cells with very high energy densities. Our approach is to genetically engineer bacteria to pump electric current in one direction, then cause the bacteria to self-assemble in series and parallel in an array to produce useful amounts of voltage and current. This approach, termed EEL (engineered electrocyte layers), should result in biofuel cells with energy densities up to 60× greater than conventional batteries. These biofuel cells should be inexpensive to produce, since the bacteria reproduce themselves, and furthermore they should be inexpensive to refuel, since the bacteria can metabolize fats, sugars, waste food, or almost any other form of organic matter. Potential applications for such refuelable, high-energy-density power sources include powering mobile electronic devices, long-lived deployable sensors, soldiers' field gear, and electric vehicles. In small-scale experiments funded by the Lincoln Laboratory New Technology Initiatives Program (NTIP), we have demonstrated some of the key principles of this approach, including engineering bacteria with suitable properties and achieving self-assembly of large numbers of bacteria.

Figure 4-1 shows the energy densities of several power sources, plotting both the energy per mass and the energy per volume. These energy densities include the conversion efficiency of each method and assume that at least 50% of the power source mass or volume is fuel. Batteries have energy densities that

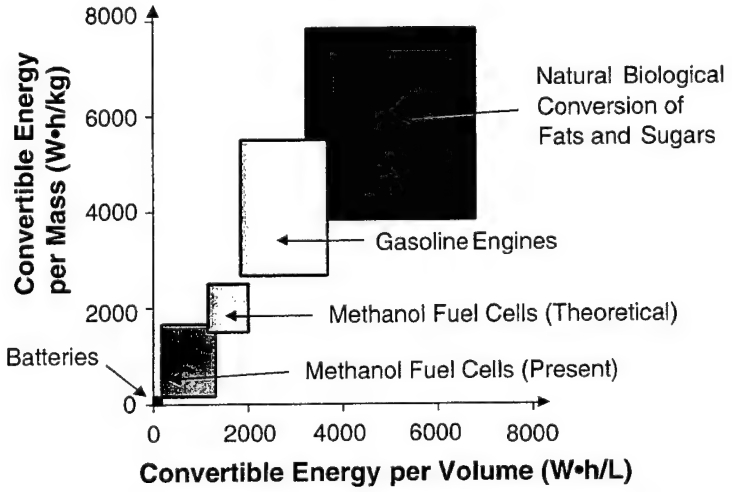

Figure 4-1. Energy capabilities of power sources. Energy densities include energy conversion efficiency, and assume ≥50% of device mass and volume is fuel.

are comparatively very low, approximately 150 W • h/kg, and they are a very mature technology which is not likely to greatly exceed this value in the foreseeable future [1]. Chemical fuel cells such as direct methanol fuel cells could potentially produce over 2000 W • h/kg, although currently they are limited to lower values by fundamental materials and design difficulties [2],[3]. Chemical fuel cells are also generally expensive and complicated to manufacture and require high operating temperatures. Gasoline engines can produce over 5000 W • h/kg, but of course their exhaust, high temperature, and noise limit their range of possible applications [4]. In contrast to these man-made power sources, natural biological systems have demonstrated the ability to convert fats, sugars, and other organic matter to electric current at almost 8000 W • h/kg and at or near room temperature [5]. The objective of this project is therefore to harness biological systems to produce electricity at very high energy densities.

As shown in Figure 4-2, our approach is to use features of two natural biological energy conversion systems. The first system is the electric eel [6],[7], which is able to generate discharges of over 500 V at approximately 1 A. The eel's current is produced in a specialized electric organ that is composed of rows and columns of electricity-producing cells, or electrocytes. Each electrocyte generates approximately 100 mV by pumping charged sodium ions unidirectionally through the cell. The electrocytes self-assemble into an organized array of cells in series and parallel, thus producing the large voltages and currents that are observed from eels. The second biological system that we hope to utilize is the cellular energy conversion process which is used by all cells from bacteria to human cells. Bacteria (or mitochondria in animal cells) convert the chemical energy of glucose, fats, and other organic matter into electrical energy by pumping protons across their membranes [8],[9]. This conversion process has a measured efficiency of approximately 75% and creates an electric potential of about 200 mV across the cell membrane. Cells normally convert that electrical energy back into chemical energy by producing molecules of adenosine triphosphate (ATP), which are then used as a chemical energy source by most cellular enzymes and functions. In the case of eel electrocytes, some of the ATP is used to power sodium ion pumps, thereby converting some of the chemical energy back into electrical energy.

Figure 4-2 shows how features of these two natural systems are incorporated into our novel fuel cell design. Using genetic engineering, we can modify the natural process by which bacteria convert chemical energy into the electrical energy of pumped protons, resulting in polar bacteria that pump protons unidirectionally. ATP production in the bacteria can be minimized so that most of their energy is available to be extracted electrically. In order to generate useful voltages and currents, the bacteria can be made to self-assemble in series and parallel in an organized structure. If the bacteria retain the measured efficiency of their natural chemical-to-electrical conversion process, the energy density of an EEL biofuel cell could be up to 60× greater than that of conventional batteries. The biofuel cell should also be inexpensive to produce (since the bacteria replicate themselves) and refuel (since it could utilize almost any organic matter for fuel).

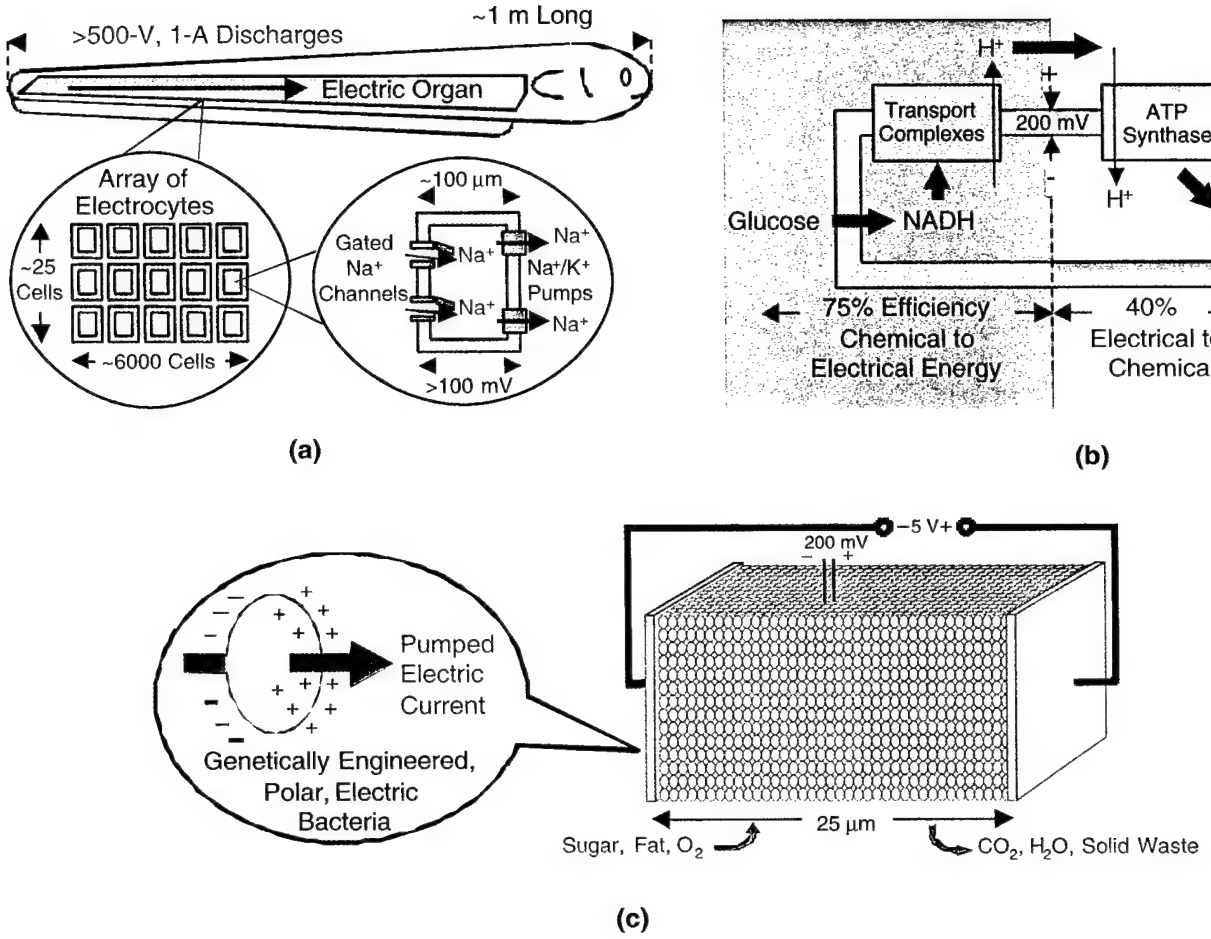

Figure 4-2. Systems of (a) the electric eel and (b) cellular energy conversion are incorporated in (c) a novel high-energy-density biofuel cell with engineered electrocyte layers.

As illustrated in Figure 4-3, we have demonstrated several key steps in the engineering of polar electric bacteria:

1. *Caulobacter crescentus* bacteria [10] were chosen as a starting point because they are already naturally asymmetric with a stalk on one end [11] and they only have proton transport in the main body, not the stalk [12],[13]. The bacteria also have holdfast adhesion molecules on the tip of the stalk [14], which should ultimately permit them all to be attached and oriented in the same direction in a biofuel cell.

2. To accent the asymmetry of the bacteria, the stalk was lengthened from ~1–2 μm to ~10–20 μm. This was accomplished by using a mutation in the bacteria's phosphate-regulation pathway and culturing the bacteria in low-phosphate medium, since the stalk is used to take up nutrient phosphate and adjusts in size as needed.

3. Next, ATP synthase was chemically inhibited to block proton reentry in the body of the bacteria. The chemical dicyclohexylcarbodiimide (DCCD) [15] is useful for this purpose, although ultimately a genetic mutation could be used. With ATP synthase inhibited, the bacteria can pump protons out through their bodies but cannot let them back in. Therefore, the bacteria can only consume ~12% of their own energy (through other pathways); the rest of the energy is available to be extracted electrically. This should also prevent excessive multiplication of the bacteria in the biofuel cell.

4. The final step is to add a proton-permeable pore to the tip of the bacterial stalk, so that the bacteria let protons in at the stalk end and pump them out at the body end. For this final step, we are using a proton pore gene from the influenza virus [16]. By splicing on the stalk-tip targeting signal from the holdfast adhesion molecules, we should be able to direct the proton pores only to the tip of the stalk in the bacteria. This step in the genetic engineering is still in progress.

As shown in Figure 4-4, we have demonstrated attachment and maintenance of *C. crescentus* on surfaces, a critical requirement for using the bacteria in a biofuel cell. Bacteria were deposited onto glass and plastic surfaces and maintained in Petri dishes of culture medium for two weeks. Four different strains of *C. crescentus* were tested (CB2A, CB15, CB15N, and YB767), and the results for the best strain (CB2A) are shown in the photographs in Figure 4-4. The photographs reveal that the bacteria formed self-organized, tightly packed monolayers on both glass and plastic surfaces. The bacterial monolayer was somewhat more organized on the glass than on the plastic, perhaps because the glass had a smoother surface than the plastic. The bacteria remained very firmly attached to the surfaces even after vigorous shaking. After about two weeks, division of the *C. crescentus* had created a cloud of new bacteria that could not find room to attach on the surface. This cloud of bacteria above the surface began to obscure the view of the bacteria on the surface. In the future, we can investigate methods of controlling bacterial overgrowth, including DCCD, bacteriostatic antibiotics, and genetic methods. Nonetheless, it is very encouraging that a closely packed monolayer of bacteria could be maintained on a surface for at least two

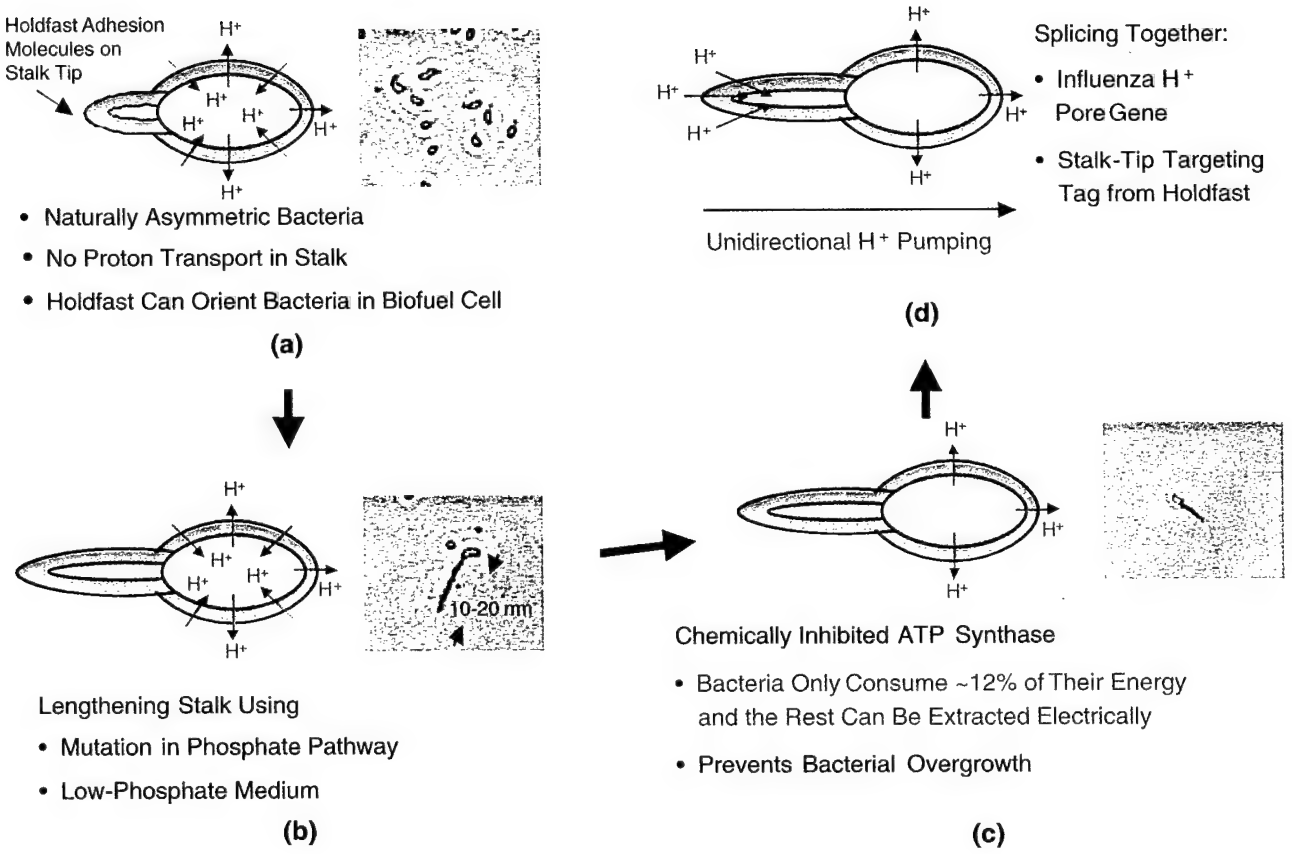

Figure 4-3. Demonstrated key steps in engineering polar electric bacteria: (a) selecting Caulobacter crescentus, (b) lengthening stalk, (c) blocking H^+ reentry, and (d) adding stalk-tip H^+ pore.

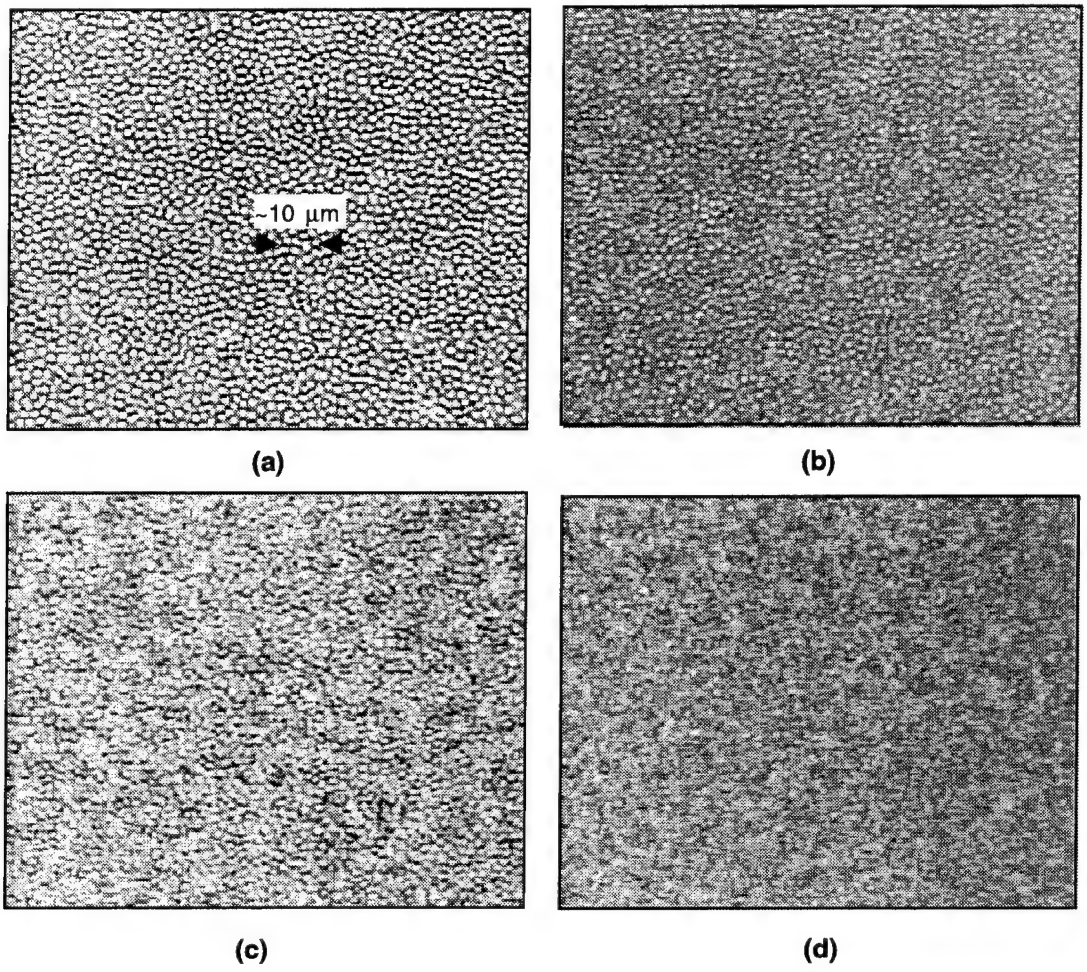

Figure 4-4. Demonstrated attachment and maintenance of C. crescentus (a) on glass after 1 day, (b) on glass after 12 days, (c) on plastic after 1 day, and (d) on plastic after 12 days. All photos were obtained with a 400× phase-contrast microscope with charge-coupled device camera.

weeks. Another important point is that it was very easy to maintain the bacteria. Their Petri dishes were simply kept at room temperature in a desk drawer in the biology laboratory, and extra culture medium was only added once during the two weeks (to prevent drying out).

To summarize, we are developing the EEL biofuel cell, a novel approach that uses genetically engineered bacteria to mimic the way electric eels produce electricity. These biofuel cells should have an energy density up to 60× greater than present batteries and could be refueled using waste food or almost any other organic matter. To prove the feasibility of this approach, we have demonstrated critical steps in engineering the bacteria, and we have shown that the bacteria can self-assemble into polar, tightly packed

monolayers and be maintained in that state for at least two weeks. In future experiments, we plan to measure the voltage difference and current flow across a monolayer of engineered bacteria.

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5. ADVANCED IMAGING TECHNOLOGY

5.1 CHARGE-COUPLED DEVICE MADE WITH A SINGLE POLYSILICON LEVEL

In a previous report we described a merged charge-coupled device (CCD) and silicon-on-insulator (SOI)–CMOS process [1] which could support the development of fully integrated image sensors comprising CCDs with integrated timing logic, clock drivers, and analog-to-digital converters. This process includes two levels of polysilicon to allow fabrication of two- or four-phase overlapping-gate CCDs. Only one of the poly levels is needed for the CMOS transistors, and the fabrication would be considerably simplified if the CCD could be made using only the CMOS poly level. Another motivation is that a single-poly CCD would not have gate overlaps, and the reduced gate capacitance of such a device would lower the clock drive power. Single-poly and single-metal CCDs were largely abandoned in the 1970s in favor of overlapping polysilicon technology, mainly because the process tools of that era were not able to routinely etch sufficiently narrow gaps between gates. Recently, there has been renewed interest in this approach, as evidenced by Japanese work [2],[3]. We describe here the results from a single-poly CCD test imager made with the CCD/CMOS process.

The CCDs in these tests have the same buried channel and dual-dielectric gate insulator as reported previously [1], but the gates were fabricated in a single poly layer. The imager comprises an imaging array of 128 × 128 pixels, each 8 × 8 μm, and a serial output register. Both imaging array and serial register are four phase with gates placed on 2-μm centers. As discussed below, the major challenge in fabricating CCDs with a single conductor level is that the gaps must be sufficiently narrow to prevent the formation of potential "pockets" or regions with higher potential beneath the gaps. These pockets trap charge and seriously degrade the charge transfer efficiency (CTE). Multiple versions of the device were designed with the various gap dimensions, the largest being nominally 0.3 μm leaving 1.7-μm-long gates. Figure 5-1 is a scanning electron micrograph of a portion of a device with 0.3-μm gaps, and shows that the gaps were successfully etched. Devices with gaps of 0.25 μm were not etched in all areas of the wafers, and gaps of 0.20 μm and smaller were not defined at all. This may seem surprising given that the lithography supports transistor gate lengths of less than 0.25 μm, but in fact it is difficult to simultaneously set the exposure and photoresist development parameters for a 0.25-μm gate length and a 0.25-μm etched gap in polysilicon.

One noteworthy feature of the merged process is that the polysilicon for the CMOS is deposited and etched before it is doped. The doping is subsequently performed by an ion implant that simultaneously forms self-aligned source and drain regions of the transistors. These implants (boron for the *p*-channel and arsenic for the *n*-channel field-effect transistors) can penetrate the exposed gate dielectric in the narrow gaps and introduce unwanted dopant into the channel, and thus the gaps must be masked from this implant. Moreover, the masking layer must be wider than the gap to allow latitude for alignment and resist exposure/development variations. As a result there is a nonimplanted lip of poly next to each gap, which for the devices described here was nominally 0.15 μm wide. It is not clear how this undoped poly would

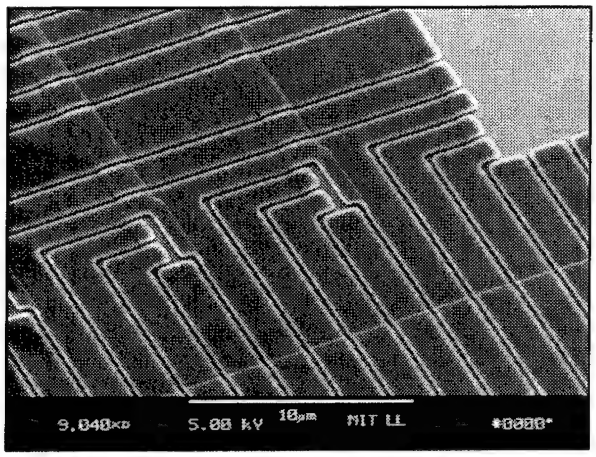

Figure 5-1. Scanning electron micrograph (SEM) of single-poly charge-coupled device (CCD) imager at the parallel-serial interface.

affect the channel electric fields that drive the charge transfer. Test structures on the wafer, however, showed that both arsenic and boron diffuse laterally more than 0.15 μm during subsequent heat treatments, so that at the end of the process the gates are doped up to the poly edges. The CCDs in this test used only As-doped gates.

A simple test of CTE was made by using the signals from bright pixel defects and noting any trailing charge as the clock voltages were varied. Figure 5-2 shows pixel amplitudes preceding and following such a pixel in the parallel transfer direction at various clock voltages and at an effective transfer rate of 130 kHz. The low rail of the clocks was 0 V in all cases. The device shows no obvious deterioration in charge transfer down to 1.8-V amplitudes. At lower voltages the well capacity drops below the amplitude of the packet, and the charge is forced to bloom into adjacent pixels. If the CTE were to degrade, the charge would bleed only into trailing pixels, but no evidence of such behavior was seen at any voltage. Figure 5-3 shows the well capacity as a function of clock swing. The CCD/CMOS process is targeted at 3.3-V clocks, and at this voltage the well capacity exceeds 100 000 e^-.

We have simulated the structure of the test imager, and the results are shown in the upper half of Figure 5-4. The gate dielectric consists of $SiO_2/Si_3N_4/SiO_2$ with thicknesses of 30/20/10 nm and the channel is formed by a phosphorus implant. The simulations illustrate the maximum empty-channel potential in the device during charge transfer from P2 into P3 and P4, as P2 is reduced in voltage from 3.3 to 0 V. Note that a pronounced pocket forms between adjacent gates set to the same bias. However, no pocket forms between P1 and P2 until P2 is close to 0 and the charge transfer out of P2 is completed. The strong lateral fields between gates at different biases effectively erase the pockets even down to a 1.1-V bias difference, in agreement with the experimental results. The lower half of Figure 5-4 shows simulations

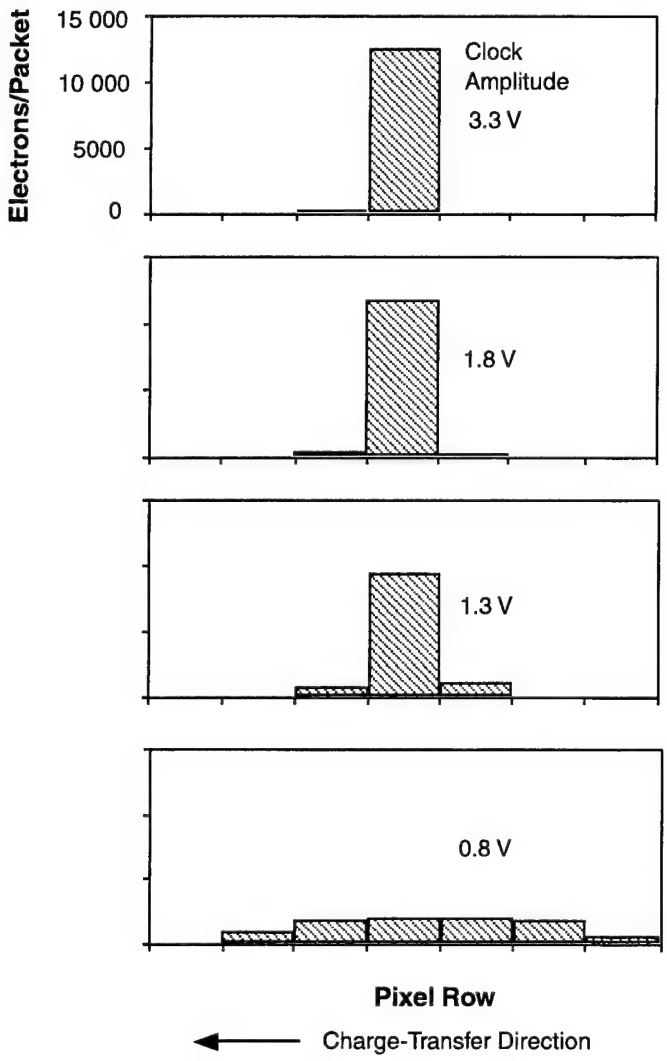

Figure 5-2. Amplitudes of charge packets originating at a bright defect in the CCD imager for various clock voltages.

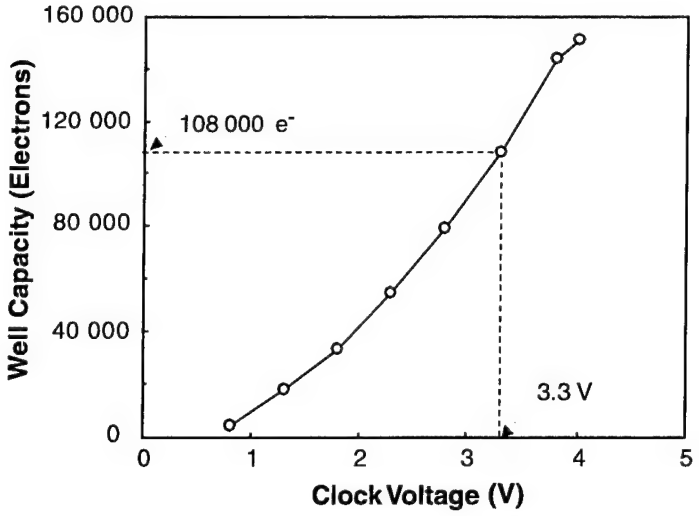

Figure 5-3. Measured well capacity of the single-poly CCD imager as a function of clock voltage.

for the case of a shallower As-doped buried channel and a thinner 10/20/10-nm gate dielectric. Here, the pockets do not disappear at the crucial gap between P1 and P2 except at clock voltages greater than 2.2 V. This latter structure is of interest because of its much higher well capacity, but it is clear that some remediation of the pocket problem will be necessary.

The origin of the pockets can be understood from a simple electrostatic model with the help of Figure 5-5. In this figure d_i is the thickness of the gate insulator and d_c is the distance from the silicon surface to the point of maximum potential in the buried channel where the electrons reside. The potential difference from channel to gate is the sum of V_c (the potential across d_c) and V_i (the potential across the insulator) where

$$V_c = \frac{qN_D d_c^2}{2\varepsilon_s} \tag{5.1}$$

and

$$V_i = \frac{qN_D d_c d_i}{\varepsilon_i} \tag{5.2}$$

Here, q is the electron charge, N_D is the buried-channel doping level, and ε_s and ε_i are the dielectric permittivities of silicon and the gate insulator. In the center of the gap region the distances d_i' and d_c' from

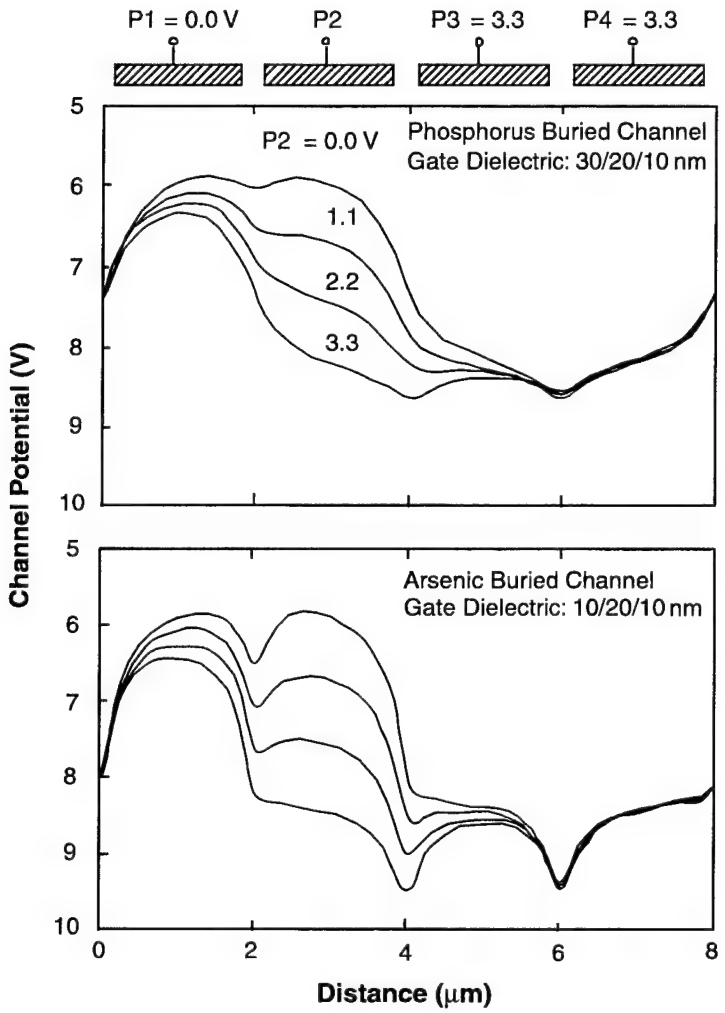

Figure 5-4. Two-dimensional simulations of channel potential in a single electrode layer CCD with 0.3-μm gaps and gates on 2.0-μm centers. The figures apply to two cases having different gate dielectrics and buried channels.

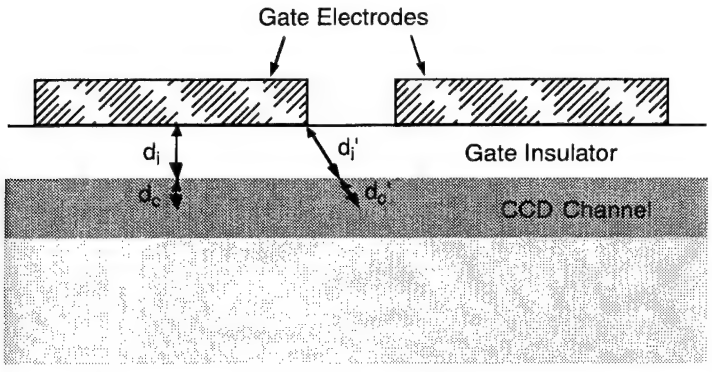

Figure 5-5. Depiction of a buried-channel CCD in a single conductor layer.

gate to channel are larger, and thus the channel-gate voltage is higher here. Clearly, as the gap is narrowed, the differences between d_i and d_i' and between d_c and d_c' are reduced, and the potential depth of the pocket will diminish. Using this simplified model, we can gain some insight into how the various device parameters influence the pocket depth by computing the difference in the gate-channel potentials ΔV beneath the gate and in the gap,

$$\begin{aligned}\Delta V &= V_c' + V_i' - (V_c + V_i) \\ &= \frac{qN_D g^2}{8\varepsilon_s} \cdot \frac{1 + \dfrac{2\varepsilon_s d_i}{\varepsilon_i d_c}}{\left(1 + \dfrac{d_i}{d_c}\right)^2}\end{aligned} \tag{5.3}$$

where g is width of the gap. This equation shows that the donor concentration and especially the gap play a direct role in determining the pocket depth, but the influence of d_i and d_c is less clear. For example, using the values for the tested CCD we find that ΔV changes less than 14% with a 2× increase or decrease in d_i or d_c. However, a change in d_c also requires an adjustment in N_D in order to maintain optimum well capacity, with N_D increasing as d_c decreases. For the case of the simulations in Figure 5-4, the surface donor concentration for the standard P buried channel was 5.4×10^{16} cm^{-3}, while for the shallow As buried channel the concentration had to be increased to 1.3×10^{17} cm^{-3}. Equation (5.3) predicts that the pocket depth will be 2.3× larger for the latter case, almost all due to the higher donor concentration. This compares with a 3.1× increase shown by the simulations, which is fairly good agreement given the simplicity of the model. This dependence on channel doping was used in the work cited in [2] and [3] to

reduce the pocket depth by implanting boron into the gaps, thus effectively reducing N_D. This method should also be effective in eliminating the pockets for the As-channel case described here.

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6. ANALOG DEVICE TECHNOLOGY

6.1 EFFECT OF IMPURITY DOPING ON THE NONLINEAR MICROWAVE SURFACE IMPEDANCE OF YBCO FILMS

Having investigated two of the proposed most likely sources of extrinsically induced nonlinearity in high-temperature superconductive YBCO thin films and concluded that neither grain boundaries [1] nor flux penetration [2] is the source, we report the effects of impurities on the nonlinear behavior. It has always been considered that nonlinearities can result from regions of suppressed order parameter [3]. Doping with impurities might introduce regions that are either normal conducting or with suppressed order parameter. In single crystals of BSCCO, zinc [4] impurities have been shown to suppress the order parameter over several atomic sites. Zinc and nickel [5] both act as strong scatterers of quasiparticles. Furthermore, Ni is magnetic, and thus shows the role of magnetic impurities. Ni and Zn have been shown to substitute for the Cu in YBCO. Doping of YBCO with calcium is also of interest because Ca is believed to substitute for the Y and provide more carriers, giving the same result as overdoping with oxygen. In addition, Ca has been shown to increase the critical current of grain boundaries [6].

To carry out these investigations we have deposited films of YBCO by laser ablation, doped with 2-at.% Ni and Zn, i.e., $YBa_2Ni_{0.06}Cu_{2.94}O_{7-\delta}$ and $YBa_2Zn_{0.06}Cu_{2.94}O_{7-\delta}$, and films with 30% Ca doping, $Y_{0.7}Ca_{0.3}Ba_2Cu_3O_{7-\delta}$, on $LaAlO_3$ substrates. Films without any impurity doping and with optimum oxygen doping were also deposited at the same time for comparison purposes. They were patterned and assembled with ground planes to form stripline resonators and measured by a technique that has been described previously [7], in which the Q and resonant frequency f_0 of the resonator are measured as a function of the microwave power at various temperatures between 4 K and T_c, and the results are converted into surface resistance $R_S(I_{rf})$ and reactance $X_S(I_{rf})$ where I_{rf} is the microwave current. The measurements were done at the fundamental frequency of 1.5 GHz.

Figure 6-1 shows the results of measurement of the low-power, linear surface resistance as a function of the reduced temperature $t = T/T_c$. The impurity-doped films show slightly lower R_S than the pure film. Overall, however, the reduction is relatively small, and there is not a dramatic effect from the inclusion of the impurities in the films.

Figure 6-2 shows the results for the nonlinear R_S at comparable values of the reduced temperatures for the various films. A very large difference in behavior is evident. The Zn- and Ni-doped films have a very substantial increase in nonlinearity relative to the reference pure film while the Ca-doped film shows only a very small increase, although the Ca doping is much higher than the Ni and Zn doping. The $R_S(I_{rf})$ of Ca-doped film is essentially unchanged from that of the pure reference film. While the magnitude of the nonlinear R_S is different, the shape of the Ni and Zn curves is similar to that of the Ca and pure films. This is demonstrated in Figure 6-3, in which the Ca- and Ni-doped films are compared by scaling the rf current for the Ni film by a factor of 3. When the current is scaled by this factor, the Ni- and Ca-doped films have

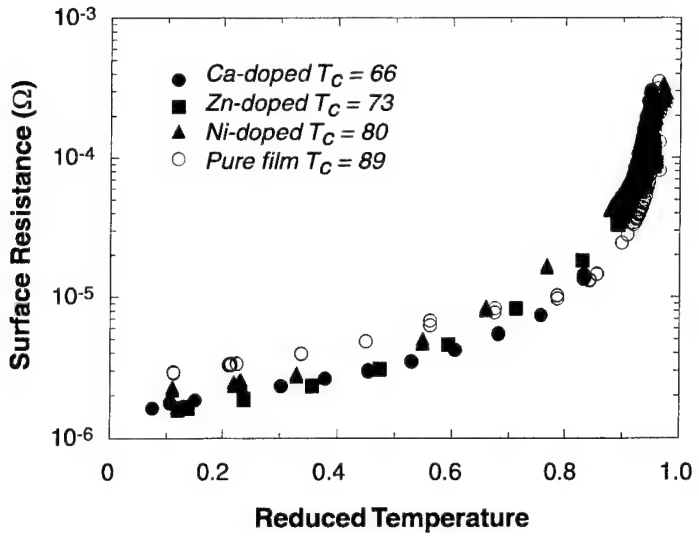

Figure 6-1. Linear, low-power surface resistance vs reduced temperature T/T_c for the impurity-doped films compared with a reference pure film. The frequency is 1.5 GHz.

comparable R_S. The agreement given when the current is scaled is a very strong indication that the mechanism of the nonlinearity is the same in all films. Similar results have been obtained with two separate sets of films, indicating that this is reproducible. A more complete presentation of the results on the impurity-doped films will be given in a publication presently in preparation [8]. Intermodulation distortion measurements also indicate that the Zn- and Ni-doped films have larger intermodulation distortion (IMD) than the pure film. Space here limits the presentation and discussion of IMD, but it will be presented elsewhere [8].

The slight reduction of the low-power linear R_S due to doping with cations is in qualitative agreement with results of R_S measurements in single crystals. It is attributed to the increase in scattering from the impurity. In the two-fluid model, the surface resistance is given by

$$R_S = \frac{\omega^2 \mu_0^2 \lambda^3 \sigma}{2} \tag{6.1}$$

where ω is the angular frequency, μ_0 is the permeability of free space, λ is the penetration depth, and σ is the real part of the conductivity which is given by

$$\sigma(T) = \frac{n_n(T) e^2 \tau(T)}{m} \tag{6.2}$$

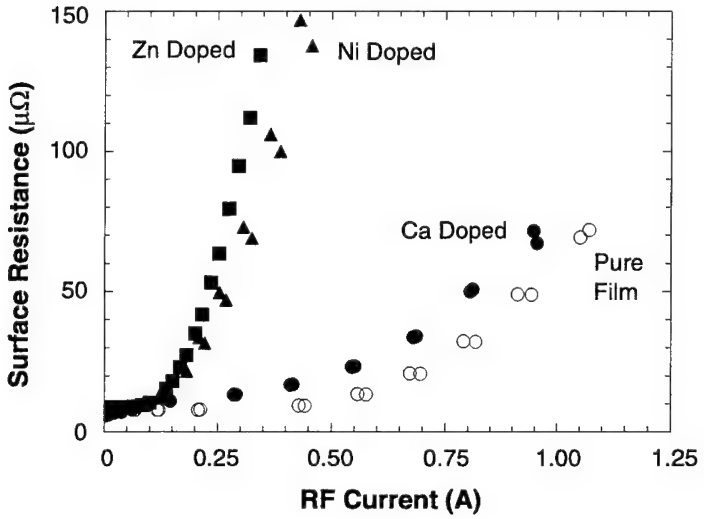

Figure 6-2. Nonlinear surface resistance vs rf current for various films at comparable reduced temperature: pure film, T_c = 90 K, t = 0.67; Ca doped, T_c = 66, t = 0.68; Ni doped, T_c = 80, t = 0.66; Zn doped, T_c = 73, t = 0.71.

where n_n is the number of normal carriers, τ is the scattering time, and m is the mass of carriers. Equation (6.1) indicates that R_S is proportional to σ, and that addition of impurities can reduce the conductivity by reducing the scattering time (increasing the scattering rate) and therefore can lead to a reduction of R_S from that of the pure material. However, the reduction of R_S is much smaller than reported for single crystals [9], most probably because films without impurity doping already contain a much larger amount of disorder than the single crystals and the addition of impurity scatters has a smaller overall effect on R_S.

Although the linear R_S is only slightly affected, the Zn and Ni doping have a large effect on the nonlinearity of R_S. As seen in Figure 6-3, the scale of the nonlinearities is increased by about a factor of 3 by the addition of these impurities, while the Ca doping has a very small effect. These results are true for the entire range of temperatures. Since the Zn and Ni are believed to substitute for the Cu, and the Ca for the Y, it seems that the nonlinearities are most likely generated by the disorder and spatial variations of the order parameter in the CuO planes or chains. The small effect from the Ca doping also suggests that cation disorder plays a very small role in the generation of nonlinear effects. Other studies [10],[11] have shown that certain kinds of structural imperfections do not degrade the microwave properties of YBCO film. It also seems that magnetic effects do not influence the nonlinearities significantly. The Ni ion appears to interact magnetically [5] while the Zn ion does not, yet the effects of the two species are indistinguishable. Both ions, however, are believed to be strong scatterers of quasiparticles and therein might lie the explanation of the effects.

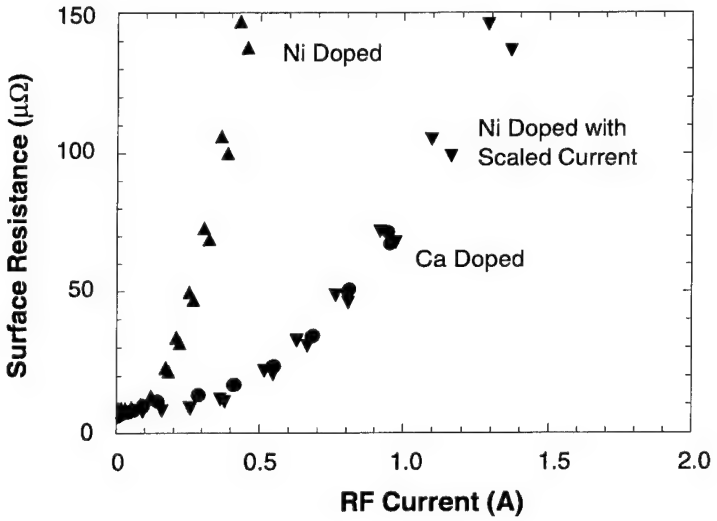

Figure 6-3. Comparison of nonlinear R_S vs current for films Ca doped, Ni doped, and Ni doped with current scaled by a factor of 3.

We have presented experimental results obtained with Ni- and Zn-impurity-doped and oxygen deficient films that show that disorder in the Cu-O planes or chains has a large influence on the nonlinear surface resistance. On the other hand, our results with Ca-doped films indicate that substitution on the Y sites seems to have little influence on the nonlinearities.

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7. ADVANCED SILICON TECHNOLOGY

7.1 DRY ETCHING OF AMORPHOUS-Si GATES FOR DEEP SUB-100-nm SILICON-ON-INSULATOR CMOS

The fabrication of deep sub-100-nm amorphous silicon (a-Si) requires fine-geometry lithography and high-fidelity etch transfer. Lincoln Laboratory requires gate definition processes to support fabrication of 25–250-nm gates for fully depleted silicon-on-insulator (SOI) circuit fabrication. Devices of this length scale have stringent processing requirements imposed by the extremely thin gate oxides and the short metallurgical junction distances. Thin SOI based devices offer performance advantages in terms of speed and power consumption [1]. This 20–40-nm layer, however, does not provide any margin should the polysilicon etch penetrate the thin gate oxide.

The optical lithography processes used to pattern the 25–100-nm gates included a double exposure with phase-shifted masks. These processes and transistor fabrication flow are detailed in previous publications [2]. This report describes the etch processes used to define the gates for sub-100-nm transistors. For sub-100-nm phase-shifted gates, thinner resist layers improve imaging characteristics such as depth of focus. Thinner resists also reduce the aspect ratio of the patterned features for improved mechanical stability of resist lines. However, the use of thinner resist places additional constraints on every etch step to be as selective to resist as possible.

The transistor configuration, shown in Figure 7-1, drives many of the gate etch integration requirements. The SOI material is thinned to 80–85 nm, and the channel region is thinned to 20–40 nm. Devices are isolated by an island etch, creating a step down to the buried oxide. Following channel implants, a 2.5–7-nm gate oxide is grown and the 120–200-nm a-Si gate is deposited. The SOI transistor topography necessitates the use of an antireflection coating (ARC) to reproducibly obtain the required resist profiles and geometries, particularly at the smaller gate lengths. Since the ARC must be etched prior to the a-Si, an in-situ ARC etch is used to simplify processing and minimize opportunities for process variation. We chose to keep with a resist mask and not to utilize an oxide hard mask to allow for easier integration with silicide formation on top of the gates for low gate resistance. The a-Si main etch process is engineered to have high selectivity to resist with sufficiently high selectivity to oxide and a clearly detectable endpoint signal so that oxide consumption is minimized prior to transitioning to the more selective overetch chemistry. The geometry of the thinned channel region increases the selectivity demands of the main etch since ion scattering from the gate and the edge of the channel can lead to oxide breakthrough during the etch at the bottom of the channel. It is critical to prevent this breakthrough, for once the oxide is consumed, the 20–40-nm channel silicon would be rapidly etched leading to open devices. The overetch chemistry must be highly selective to oxide as a significant overetch is required to prevent stringer formation over the device topography. Ultrathin 2.5-nm gate oxides, used in highly scaled transistors, place additional importance on the selectivities required. Finally, the resist strip following gate

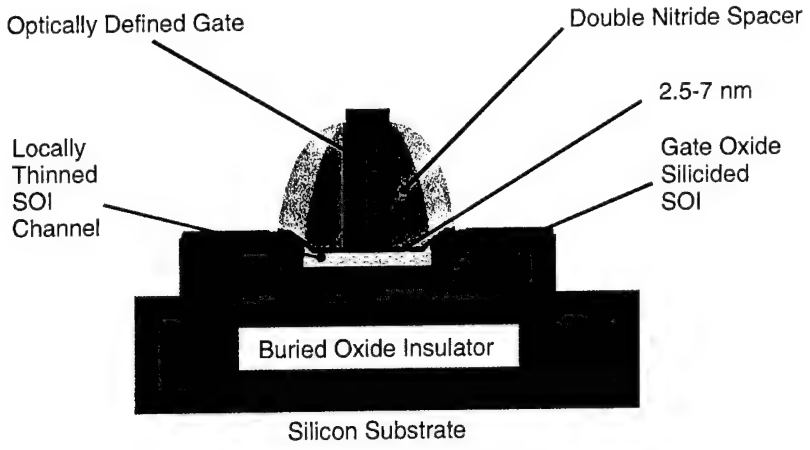

Figure 7-1. Schematic diagram of silicon-on-insulator (SOI) transistor.

etch must neither attack the gate oxide nor damage the high aspect ratio gates; these requirements mean that HF-free chemistries must be used for stripping without any megasonic agitation. Stripping the etch residues was a consideration when developing the etch process.

The transistor fabrication continues with nitride spacer formation. The first thin nitride spacer provides masking for gate extension implants, and the second thicker spacer prevents silicide formation in the thinned channel regions, which could consume the silicon and lead to high resistance or open devices. The nitride spacers also provide mechanical stability for high aspect ratio devices. Following source/drain implants and salicide formation on the gates and source/drain regions, a three-level metal backend completes the circuit fabrication process. This three-level metal backend requires the use of chemical mechanical planarization (CMP) both to planarize oxide dielectrics between the metal levels and to damascene the tungsten plugs that fill the contact and via holes connecting the metal layers. To achieve planar surfaces between the devices, dummy poly fill patterns are placed in open areas. Such fill increases poly mask density from 1–5% actual gate device area to 15–40% gate mask area, placing additional challenges on endpoint detection for the gate etch.

To summarize, the etch and integration requirements for defining a-Si gates for sub-100-nm circuit fabrication are (1) critical dimension (CD) values of 25–250 nm, uniformity of ±10%, and etch bias of ±10 nm; (2) vertical etch profiles; (3) integrated ARC etch; (4) endpoint determination in main etch to minimal gate oxide for 15–40% mask area; (5) selectivity to oxide etch in overetch greater than 100:1; and (6) ability to completely strip all etch and resist residues.

We have developed a process that meets these etch and integration requirements for defining sub-100-nm a-Si gates using a LAM 9400 transformer coupled plasma (TCP) high density plasma etch tool. Gates are patterned using optical lithography with a Canon EX-4 248-nm stepper which has a

TABLE 7-1
Gate Definition Process Parameters

Step	ARC Main Etch	Breakthrough Etch	Poly Main Etch	Poly Overetch
Pressure (mtorr)	4	4	10	60
TCP Source Power (W)	200	200	200	250
Bias Power (W)	50	100	100	100
Chemistry	$Cl_2/HBr/O_2$	Cl_2	$Cl_2/HBr/He/O_2$	$HBr/He/O_2$
Etch Rates (nm/s)				
AR3	3.6			
UV5	1.94		0.6	
Thermal Oxide			0.13	0.001
a-Si			2.6	1.46
Selectivity from Blanket Wafers				
ARC:Resist	1.9:1			
Poly:Oxide			20:1	1500:1
Poly:Resist			4.5:1	

numerical aperture (NA) of 0.6 and a partial coherence of 0.3. Gates are etched with a LAM 9400 TCP etch tool. Low-pressure operation and independent control of substrate bias in this high density plasma etch tool allow for anisotropic etching [3]. The LAM 9400 TCP has independently controlled TCP source and wafer rf bias powers at 13.56 MHz. A single 150-mm wafer is held with an electrostatic chuck at 45°C with fluid cooling and a helium back side pressure of 8 Torr for efficient heat transfer between the chuck and the wafer. Prior to etching gates, the chamber is conditioned with two blanket a-Si wafers. The multistep etch process consists of an ARC etch, a chlorine breakthrough, an $HBr/Cl_2/He/O_2$ endpointed main etch, and an $HBr/He/O_2$ overetch; significant etch parameters are included in Table 7-1.

The gates are defined using a double-exposure phase-shift method [4] with 100-nm AR3™ coating and 255–395-nm UV5™ Shipley resist. Interactions between the resist and the ARC can lead to formation of an anti-footing at the base of the resist as shown in the top two scanning electron micrographs (SEMs) in Figure 7-2. This narrowing of the resist feature at its base is caused by photoacid additives included in the ARC to prevent footing formation. Cross sections of resist lines showed this anti-footing to be significant at smaller geometries. This interaction was minimized by the use of a high-temperature ARC bake at 215°C prior to spinning the resist, as shown in Figure 7-2. Resist profiles can be transferred into the etch

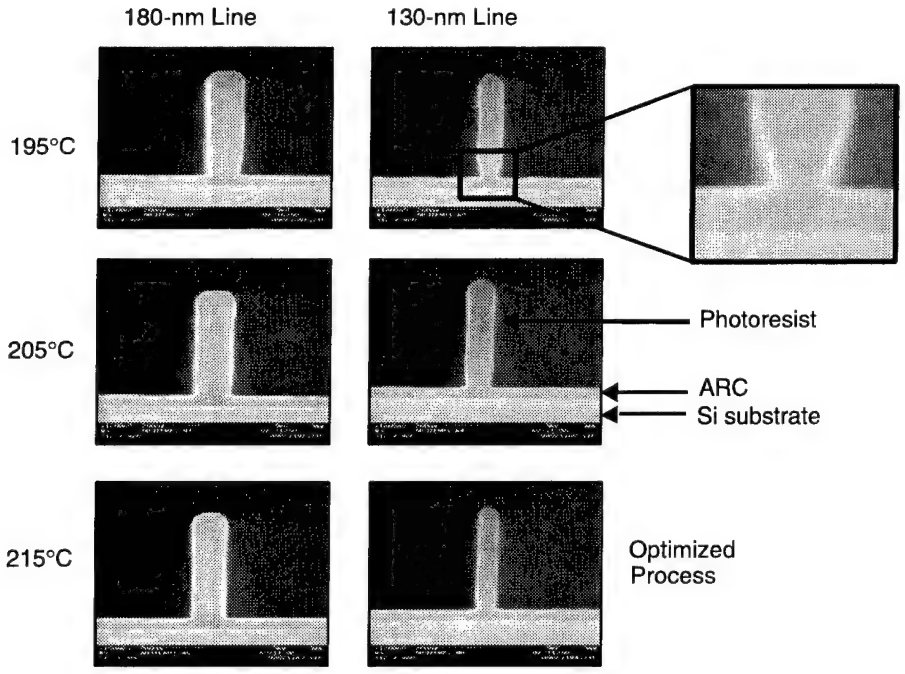

Figure 7-2. Scanning electron micrographs showing that high-temperature antireflection coating bake minimizes resist footing.

and become confused with change in CD during etch (etch bias) when CDs are measured using top down SEM images only. We used cross sections of wafers both after resist patterning and after etch to optimize the etch processes for minimal change in CD during etch.

Our ARC etch was optimized to maintain gate CD and minimize resist loss. Since the chemistries of the ARC and the resist are quite similar, ARC:resist etch rate selectivities much greater than 1:1 are difficult to achieve and the as-spun resist thickness must tolerate some loss during the ARC etch step. Cross sections of ARC etched features using several different etch gas chemistries, including mixtures of $Cl_2/HBr/O_2$, Cl_2/O_2, and N_2/O_2, were examined. A mixture of $Cl_2/HBr/O_2$ at 4 mtorr with a source power of 200 W, a bias power of 50 W, and lower electrode temperature of 45°C was found to best maintain CD and maximize selectivity to resist. The addition of the HBr to the gas mixture helped maintain resist and ARC pattern profile following the ARC etch. In the absence of significant ion bombardment, the etch rates of resist in HBr plasmas are significantly less than the etch rates of resist in Cl and O_2 based plasmas [5]. We hypothesize that the addition of HBr to the gas mixture increased the importance of the physical sputtering of the ions in the high density plasma, reducing the lateral etch rate relative to the vertical etch rate giving better CD and profile control. The addition of HBr to the gas mixture also improved the ARC:UV5 selectivity from 1.4:1 for the Cl_2/O_2 etch gases to 1.9:1 for $Cl_2/HBr/O_2$ etch gases. The hydroxystyrene based resist etch rate was reduced by one-third while the etch rate of the polyacrylate

based ARC was only slightly reduced giving a significant improvement in selectivity; the exact mechanism for this is not completely understood. We obtained ARC etch rates of 3.6 nm/s and resist etch rates of 1.9 nm/s. The ARC etch endpoint is triggered by a reduction in the optical emission signal at 520 nm, which is characteristic for CO emission. A 30–50% ARC overetch with the same power and chemistry follows to remove ARC from low regions in the wafer topography, which have thicker ARC coatings owing to planarization when the ARC is spun on the wafer. Even with the selectivities we achieved, etching 100 nm of AR3 consumes 81 nm of resist, placing additional burdens on the a-Si etch, particularly for sub-100-nm features defined with only 255 nm of resist.

A short Cl breakthrough etch at 4 mtorr with a source power of 200 W and a bias power of 100 W is used to remove any native oxide on the surface of the a-Si. Since the main etch is selective to oxide, even a thin layer of remaining oxide would interfere with the a-Si etch.

The a-Si main etch was developed based on LAM's recommended recipe using a chemistry of Cl_2/HBr/He/O_2 at a TCP source power of 200 W. Low-pressure operation at 10 mtorr and a bias power of 100 W were selected to maintain vertical profiles. Device requirements for selectivities and CD control dictate the choice of main etch chemistry. Cl plasmas etch silicon rapidly but do not provide sufficient selectivity to either resist or oxide, and HBr plasmas have a low Si etch rate but improve the selectivity to both resist and oxide; the HBr/Cl_2 mixture gives high silicon etch rates with satisfactory selectivities [6],[7]. Small additions of oxygen improve the selectivity to oxide in both the main etch and in the overetch [8], and He is included to improve the uniformity of the etch. The percent O_2 in the gas mixture was optimized at 0.8% to maximize etch rate selectivity of a-Si to thermal oxide while minimizing resist loss. Etch rates of 2.6 nm/s for a-Si with a standard deviation of 2% were obtained, while the etch rate for thermal oxide was 0.13 nm/s giving a selectivity of 20:1 for a-Si:oxide. Resist etch rates in the largely HBr plasma were low, 0.58 nm/s, giving a selectivity of 4.5:1 for a-Si:resist; this selectivity meets the process demands as an 80-s etch would consume only 50 nm of resist.

We found that temperature was an important parameter for optimizing our CD change with etch; higher temperatures led to decrease in CD while lower temperatures caused excessive CD growth due to polymer deposition during etch, which is consistent with previous studies of poly-Si etching with HBr [9]. Examination of cross sections for samples etched at temperatures from 25 to 65°C showed excessive notching at the base of the etched a-Si lines at the higher temperatures, presumably owing to inadequate polymer formation during the main etch to prevent lateral etching by Cl during the transition to the overetch. A lower electrode temperature of 45°C was chosen as a good compromise for minimal change in CD with minimal notching. Accurate endpoint determination for the completion of the a-Si etch is critical to preserving thin gate oxides. More details about the endpoint determination are given below.

For increased selectivity to oxide, the overetch chemistry eliminates the Cl and increases the HBr while maintaining O_2 at an increased pressure of 60 mtorr. Very high selectivity (1500:1) was obtained when measuring etch rates of blanket a-Si and thermal oxide wafers. The oxide etch rate in the presence of a resist mask is higher than measured for blanket films as the resist mask contributes carbon to the plasma which increases the oxide etch rate [10]. Adequate selectivity to oxide has been confirmed by ellipsometer measurements of oxide thickness remaining after the a-Si etch on patterned wafers. From ellipsometry

data, the oxide removed during the time taken to determine the endpoint of the main etch followed by a 100-s overetch is 2.0 nm ± 0.5 nm. The long overetch is required to remove all a-Si from the steps created by the SOI isolation etch. These steps can be up to 90 nm, and the etch rate of a-Si in the overetch is 1.5 nm/s. Even with the long overetch, SEM cross sections confirm that we have not broken through the gate oxide for devices fabricated with 2.5-nm gate oxides. To extend the technology to gate oxides thinner than 2.5 nm we will need to develop a more selective landing step to switch to before the main etch has cleared the a-Si.

This choice of plasma etch chemistry and operating temperature result in an etch without excessive sidewall buildup of either polymer or SiX_xO_y (where X is either Cl or HBr) as seen elsewhere [11], and we are able to strip in standard ACT-1TM, piranha, and SC1 chemistries. We have found that with high aspect ratio gate features, megasonic cleans must be avoided prior to spacer formation in order to maintain mechanical stability of the gates. No HF dips are required here to clean up etch residues; HF dips would not be compatible with process integration since these would attack the thin gate oxide. We propose that the mechanism for the anisotropy in our gate etch process is more closely related to that proposed by Cheng et al. [12] due to the high concentration of HBr in the etch and the optimization of our oxygen percentage in both the main etch and the overetch to less than 1%. As-etched and stripped a-Si lines are shown in Figure 7-3.

A change in poly main etch endpoint detection was required for integration into our current CMOS flow. We detected endpoint for our previous process using the falling 520-nm SiCl etch product optical signature. Current generations of CMOS flows require polysilicon dummy "fill" in the field regions in order to maintain adequate planarity in the CMP process. As shown in Figure 7-4, this fill increases the area of the resist mask considerably (from 1–5% to 11–40%). Etching of this increased area of resist mask

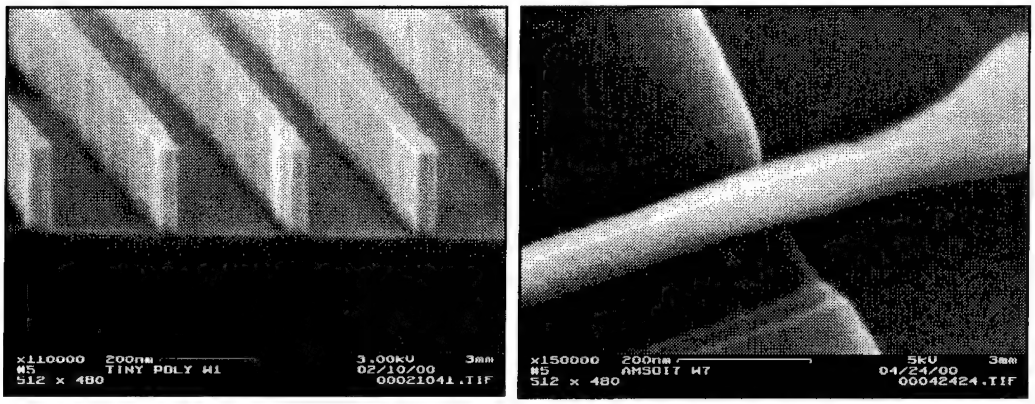

Figure 7-3. Tilted views of as-etched and stripped a-Si lines both stopping on 4-nm gate oxide: (a) 36-nm grating on a 250-nm pitch and (b) 25-nm transistor. The waviness of the 36-nm line is a direct transfer of a lithography pattern artifact.

generates CO during the poly etch which interferes with the 520-nm signature, thus giving inadequate endpoint response for stopping on thin gate oxides. Optical emission signals for wafers etched without poly fill (5% mask density), and with the addition of poly fill (15% mask density) at 520 nm (8-nm bandwidth), are shown in Figure 7-5. With the higher mask density the optical emission signal remains high for the full extent of the allotted main etch time, thus failing to trigger the endpoint of the etch.

Shown in Figure 7-6 are persistent optical emission lines at 510 and 520 nm [13]. We changed our optical emission filter to 510 nm (8-nm bandwidth), intending to monitor the falling SiCl signature at that wavelength without interference from CO signals. What we found instead, corresponding to the clearing of our a-Si film over oxide, was a strong rise in the 510-nm signal, which we assume corresponds to the rising signature of the Cl_2^+ reactant gas. Optical emission traces for channel A (520 nm) and B (510 nm) are shown in Figure 7-7. We have implemented this endpoint method, which gives rapid response to stop on 2.5-nm gate oxides.

Vertical etch profiles with minimal etch-induced line edge roughness have been obtained for linewidths down to 25 nm, stopping on thin gate oxides down to 2.5 nm. Cross sections of completed poly gates on locally thinned SOI islands with gate lengths of 50, 25, and 9 nm are shown in Figure 7-8. The samples were HF decorated to enhance image clarity. Note the vertical profiles obtained, with the slight narrowing at the base occurring during the 100-s overetch. No gate oxide breakthrough has occurred, as evidenced by the continuous SOI channel. Functional devices [2] obtained at gate lengths of 25 and 50 nm are shown in Figures 8(a) and 8(b). Figure 8(c) shows a very high aspect ratio 9-nm gate with a vertical profile and $COSi_2$ visible on the top of the gate. The etch process discussed allows us to fabricate SOI-CMOS devices with gate lengths specified by the 2000 *International Technology Roadmap for Semiconductors* for the 35-nm node, called for in 2013 [14].

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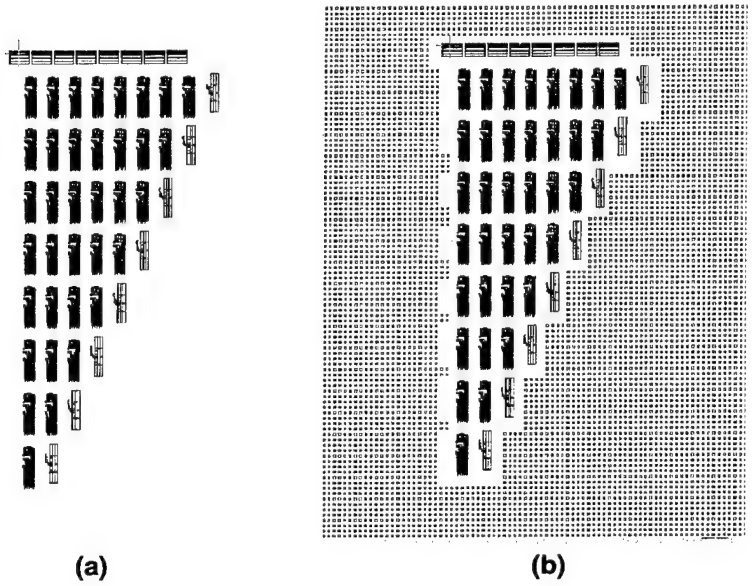

Figure 7-4. 16-bit multiplier gate pattern (a) without fill and (b) with the addition of fill to maximize planarity following backend dielectric chemical mechanical planarization.

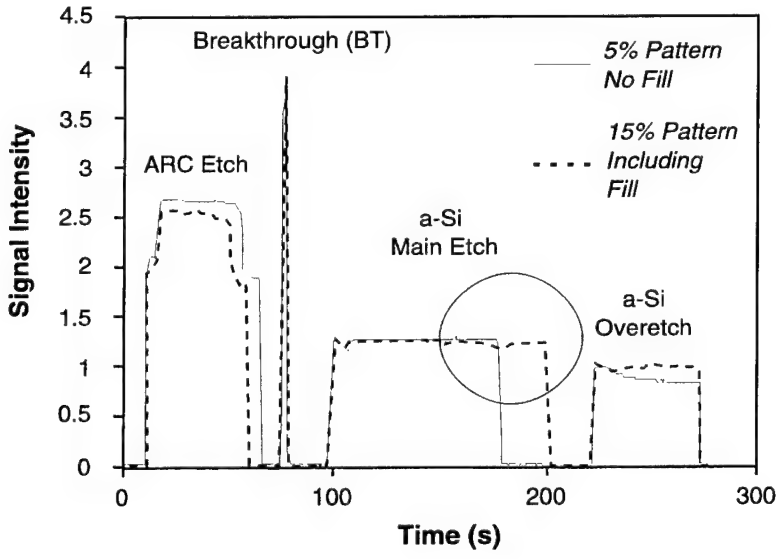

Figure 7-5. Optical emission signal at 520 nm for etch of patterned wafers with mask densities of 5 and 15%.

Wavelength	Name	Intensity	
503.11	SiCl	8	
504.01	BO	9	
505.27	CO	8	
506.2	Ar^+	0.7	
506.466	Ti	2	
508.08	**Cl_2^+**	**7**	
508.4	**SiCl**	**8**	
508.582	Cd	6	
510.2	AlO	6	Species Detected by 510-nm Filter Channel B
510.555	Cu	4	
512.31	AlO	6	
513.64	N_2^+	5	
514.2	Ar^+	0.5	
515.326	Cu	4	
516.22	**SiCl**	**8**	
516.52	**C_2**	**10**	
519.298	Ti	2	
519.82	**CO**	**10**	
521.039	Ti	2	Species Detected by 520-nm Filter Channel A
521.82	Cu	5	
521.83	**SiCl**	**8**	
522.006	Cu	4	
523.4	O_2^+	9	
524.1	O_2^+	8	
525.1	O_2^+	10	
525.9	O_2^+	6	
526.78	AlCl	10	

Figure 7-6. Persistent optical emission lines at 510 and 520 nm.

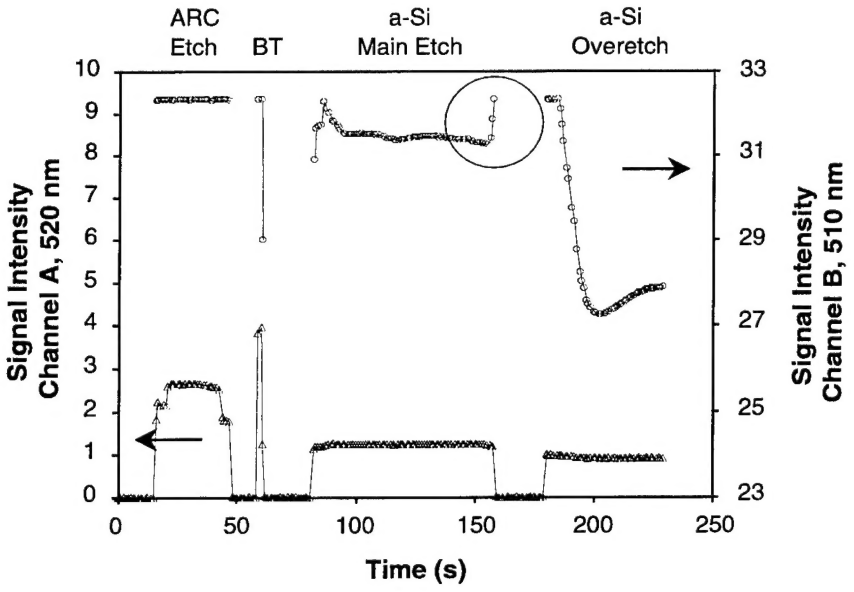

Figure 7-7. Optical emission signal at 510 and 520 nm for etch of patterned wafer with mask density >15%.

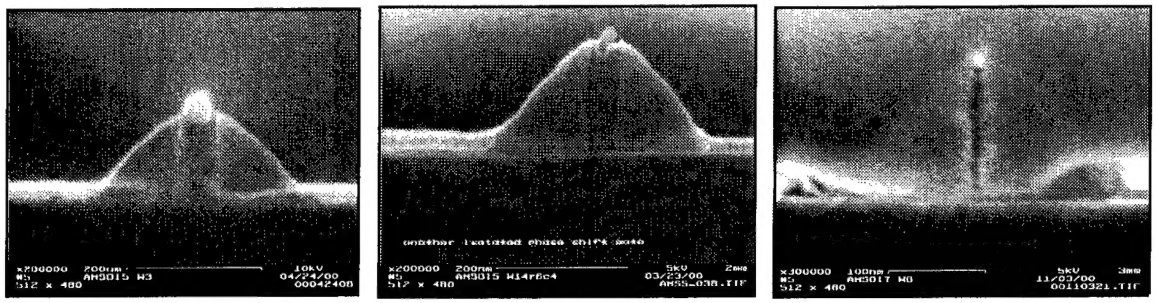

Figure 7-8. Cross sections of completed polysilicon gates on locally thinned SOI islands: (a) 50 nm, (b) 25 nm, and (c) 9 nm.

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13. ABSTRACT (*Maximum 200 words*)

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May–31 July 2001. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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